November 2011

AR9271 Single-Chip 1x1 MAC/BB/Radio/PA/LNA with USB Interface for 802.11n 2.4 GHz WLANs

General Description

The Atheros AR9271 is a highly integrated single-chip solution for 2.4 GHz 802.11n-ready wireless local area networks (WLANs) that enables a high-performance 1x1 configuration for wireless station applications demanding robust link quality and maximum throughput and range. The AR9271 integrates a multi-protocol MAC, baseband processor, analog-to-digital and digital-to-analog (ADC/DAC) converters, 1x1 radio transceiver, RF switch, and USB interface in an all-CMOS device for low power and small form factor applications.

The AR9271 implements half-duplex OFDM, CCK, and DSSS baseband processing, supporting 72.2 Mbps for 20 MHz and 150 Mbps for 40 MHz channel and IEEE 802.11b/g data rates. Other features include signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. The AR9271 MAC supports the 802.11 wireless MAC protocol, 802.11i security, receive and transmit filtering, error recovery, and quality of service (QoS).

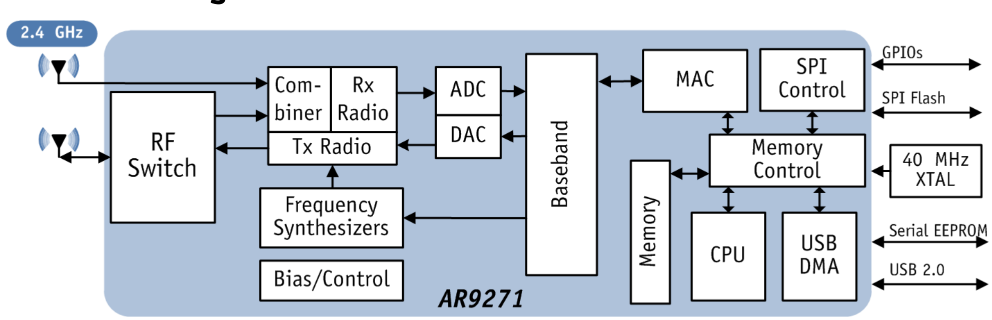
The AR9271 supports one transmit traffic stream and one receive traffic stream using one integrated Tx chain and one receive chain for high throughput and range performance. The Tx chain combines baseband in-phase (I) and quadrature (Q) signals, converts them to the desired frequency, and drives the RF signal to the antenna. The frequency synthesizer supports frequencies defined by IEEE 802.11b/g/n specifications.

The AR9271 supports frame data transfer to and from the host using a USB interface that provides interrupt generation/reporting, power save, and status reporting. Other external interfaces include serial EEPROM and GPIOs. The AR9271 is interoperable with standard legacy 802.11b/g devices.

Features

- All-CMOS solution interoperable with IEEE 802.11b/g/n WLANs
- Intergrated RF front end with high-output PA, LNA, Rx/Tx switch
- Internal diversity switch which selects antenna 1 or 2 for baseband signal processing
- Supports optional external LNA, PA
- 2.4 GHz WLAN MAC/BB processing
- BPSK, QPSK, 16 QAM, 64 QAM, DBPSK, DQPSK, and CCK modulation schemes
- Supports 72.2 Mbps for 20 MHz and 150 Mbps for 40 MHz channel operations
- Wireless multimedia enhancements quality of service support (QoS)
- 802.11e-compatible bursting
- Support for IEEE 802.11e and IEEE 802.11i standards
- WEP, TKIP, and AES hardware encryption
- Reduced (short) guard interval
- Frame aggregation
- Block ACK
- USB 2.0 interface
- Supports the access of a serial peripheral (SPI) compatible Flash memory, which includes booting from an SPI Flash and auto-installation
- IEEE 1149.1 standard test access port and boundary scan architecture supported
- 68-pin, 8 mm x 8 mm LPCC package

AR9271 System Block Diagram



© 2010-11 by Atheros Communications, Inc. All rights reserved. Atheros®, Atheros Driven®, Align®, Atheros XR®, Driving the Wireless Future®, Intellon®, No New Wires®, Orion®, PLC4Trucks®, Powerpacket®, Spread Spectrum Carrier®, SSC®, ROCm®, Super A/G®, Super G®, Super N®, The Air is Cleaner at 5-GHz®, Total 802.11®, U-Nav®, Wake on Wireless®, Wireless Future. Unleashed Now.®, and XSPAN®, are registered by Atheros Communications, Inc. Atheros SST™, Signal-Sustain Technology™, Ethos™, Install N Go™, IQUE™, ROCm™, amp™, Simpli-Fi™, There is Here™, U-Map™, U-Tag™, and 5-UP™ are trademarks of Atheros Communications, Inc. The Atheros logo is a registered trademark of Atheros Communications, Inc. All other trademarks are the property of their respective holders. Subject to change without

Revision History

Ver.	Date	Description
1.0	March 2011	Initial release
2.0	November 2011	Updated Table 8-1 D2/E2 dimensions, nominal from 5.49 to 5.84 mm, maximum from 5.64 to 6.35 mm. Added sawed-type package diagram and dimensions, Figure 8-2 and Table 8-2.

Table of Contents

1. Pin Descriptions

This section contains a package pinout (see Figure 1-1 and Table 1-1) and a tabular listing of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

I	Digital input signal
I/O	A digital bidirectional signal
IA	Analog input signal
IA/OA	Analog bidirectional signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
O	A digital output signal
OA	An analog output signal
OD	A digital output signal with open drain
P	A power or ground signal

Figure 1-1 shows the LPCC-68 package pinout.

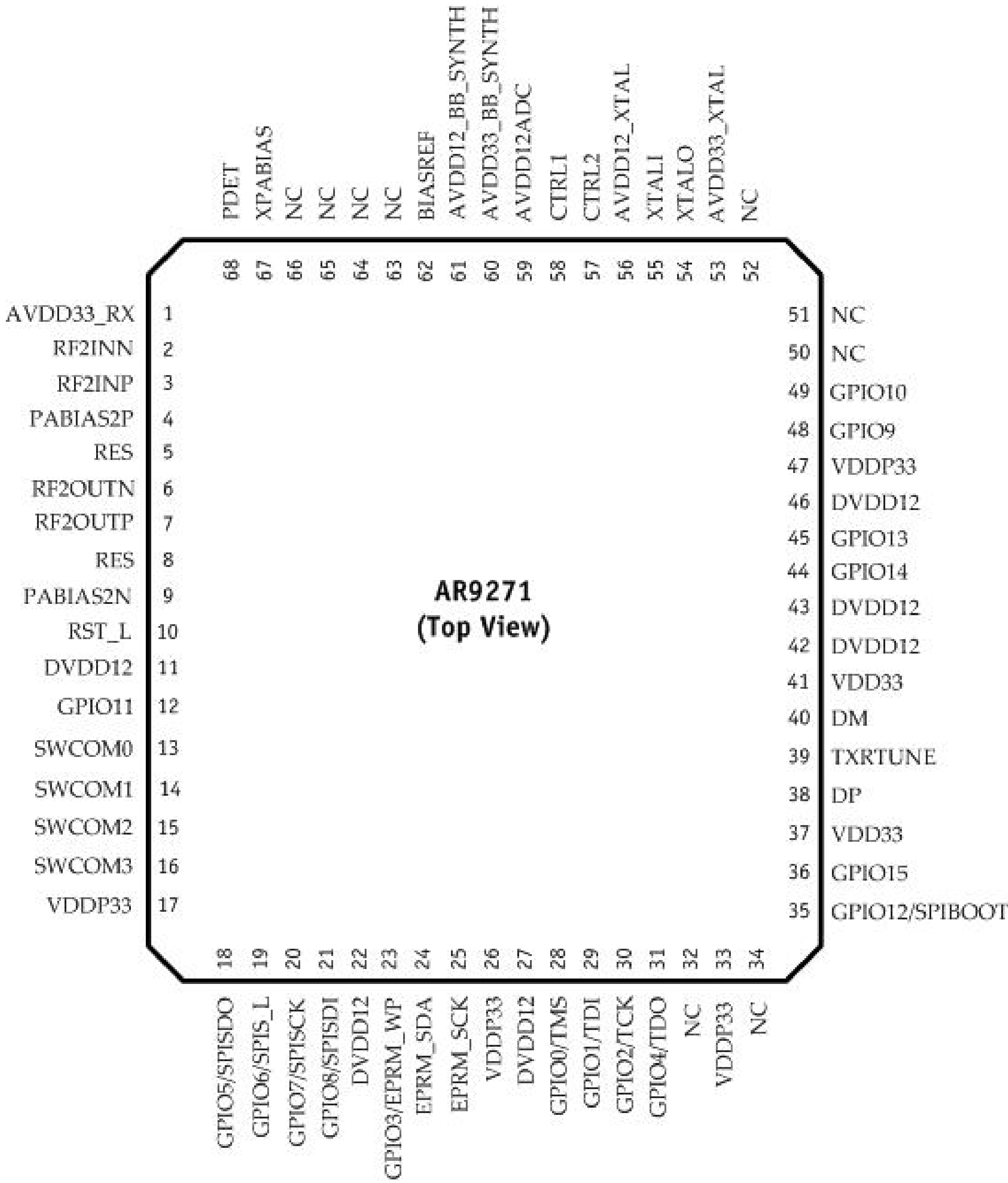


Figure 1-1. **LPCC-68 Package Pinout**

Table 1-1. **Signal-to-Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
USB Pins			
TXRTUNE	39	IA/OA	Transmitter Resistor Tune Pin. Connects to an external resistor of 51 Ω that adjusts the USB 2.0 PHY high-speed source impedance.
DM	40	IA/OA	USB D- Signal. Carries USB data to and from the USB 2.0 PHY
DP	38	IA/OA	USB D+ Signal. Carries USB data to and from the USB 2.0 PHY
Radio			
BIASREF	62	IA	BIASREF voltage is 310 mV; must connect a 6.19 KΩ ± 1% resistor to ground
RF2INN	2	IA	Differential RF inputs. Use one side for single-ended input.
RF2INP	3	IA	
RF2OUTN	6	IA/OA	Differential RF power amplifier output. Differential RF input for antenna 1. The RF amplifier output only appears on antenna 1. There is a diversity switch inside the AR9271 that selects antenna 1 or antenna 0 for baseband signal processing. There is also a Tx/Rx switch for antenna 1.
RF2OUTP	7	IA/OA	
Analog Interface			
PABIAS2N	9	IA	Bias voltage for internal PA
PABIAS2P	4	IA	
PDET	68	IA	Input for optional external power detector
XPABIAS	67	OA	Bias for optional external power amplifier
External Switch Control			
SWCOM0	13	O	Common switch control
SWCOM1	14	O	
SWCOM2	15	O	
SWCOM3	16	O	
General			
RST_L	10	IH/OD	Reset for the AR9271. This pin has an active open drain pull down that forces it low if either the core or the IO supply is below safe operating limits.
XTALI	55	I	40 MHz crystal.
XTALO	54	O	
GPIO			
GPIO0/TMS	28	I/O	General purpose and multiplexed for JTAG test mode
GPIO1/TDI	29	I/O	General purpose and multiplexed for JTAG data input
GPIO2/TCK	30	I/O	General purpose and multiplexed for JTAG test clock
GPIO4/TDO	31	I/O	General purpose and multiplexed for JTAG data output
GPIO5/SPISDO	18	I/O	General purpose and multiplexed serial output data from an SPI device
GPIO6/SPIS_L	19	I/O	General purpose and multiplexed serial interface enable signal of SPI

Table 1-1. **Signal-to-Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
GPIO7/SPISCK	20	I/O	General purpose and multiplexed serial clock to SPI device
GPIO8/SPISDI	21	I/O	General purpose and multiplexed serial input data from an SPI device
GPIO9	48	I/O	General purpose pins
GPIO10	49	I/O	
GPIO11	12	I/O	
GPIO12/SPIBOOT	35	I/O	If this pin is tied to high at power on, the system will boot from an external SPI Flash instead of the internal ROM
GPIO13	45	I/O	General Purpose Pins
GPIO14	44	I/O	
GPIO15	36	I/O	
Serial EEPROM			
GPIO3/EPRM_WP	23	I/O	Serial EEPROM write protection control output and multiplexed as a general purpose pin
EPRM_SDA	24	I/O	Serial EEPROM data
EPRM_SCK	25	O	Serial EEPROM clock output

Symbol	Pin	Description
Power		
VDD33	37, 41	Analog 3.3 V power supply for USB PHY
VDDP33	17, 26, 33, 47	Digital 3.3 V power supply
DVDD12	11, 22, 27, 42, 43, 46	Digital 1.2 V power supply
AVDD33_RX	1	Analog 3.3 V power supply
AVDD33_XTAL	53	Analog 3.3 V power supply
AVDD12_XTAL	56	Analog 1.2 V power supply
AVDD12ADC	59	Analog 1.2 V power supply
AVDD33_BB_SYNTH	60	Analog 3.3 V power supply
AVDD12_BB_SYNTH	61	Analog 1.2 V power supply
Ground Pad		
Exposed Ground Pad	—	Tied to GND (see “Package Dimensions” on page 147)
Control		
CTRL1	58	Used to drive the external PNP device. Connect the base of the external PNP to CTRL1
CTRL2	57	Used to drive the LDO output. Connect the collector of the external PNP here
No Connection		
NC	32, 34, 50, 51, 52, 63, 64, 65, 66	No connect
Reserved		
RES	5,8	Reserved, can be left open or optionally connected to AVDD33

2. Functional Description

2.1 Overview

The AR9271 consists of five major functional blocks: CPU, USB 2.0, MAC, digital PHY, and radio.

The IEEE 802.11 MAC functionality is partitioned between the host and the AR9271. IEEE 802.11 MAC data service is provided by the MAC of the AR9271, while the host software, with the aid of the AR9271 MAC, controls Tx and Rx queue processing.

The baseband digital processing functions are implemented by the digital PHY of the AR9271. The radio frequency (RF) and baseband analog processing are provided by the integrated radio. The physical layer (PHY) is partitioned between the baseband processor and the radio. The configuration block, Data RAM, PLL, ADC, DAC, EEPROM interface, JTAG, antenna control, LED and GPIO complete the AR9271 functionality. See Figure 2-1.

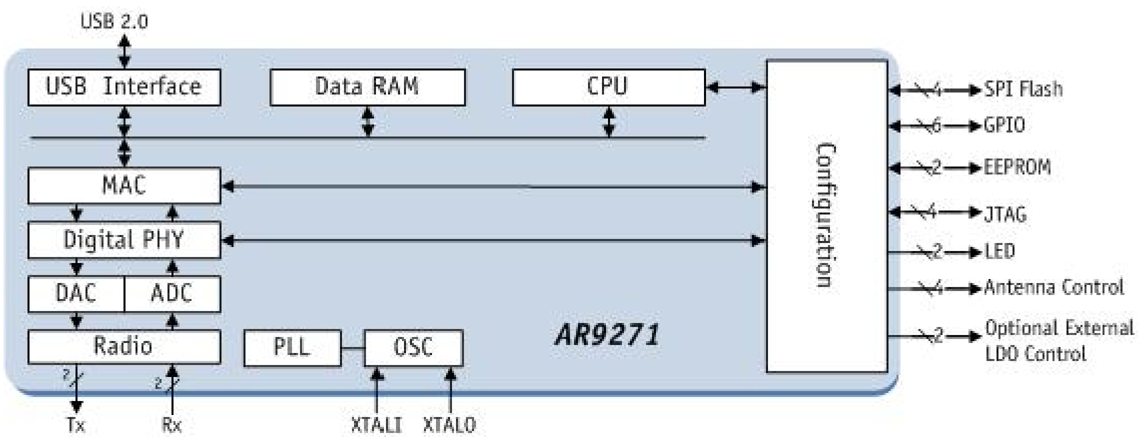


Figure 2-1. **Functional Block Diagram of the AR9281**

2.1.1 Configuration Block

The configuration block provides control, status, and configuration, for each major functional block. This block contains registers accessed by other blocks and by the host using the USB interface. See "Register Descriptions" on page 37 for more information.

2.1.2 AR9271 Address MAP

Internal registers of the various functional blocks and the AR9271 peripheral interface are accessible with the host using the USB interface. These register locations are defined as offset addresses. The combination of the host base address and the offset address allows access to a particular internal register. Table 2-1 lists the offset addresses for the AR9271 internal registers and peripheral interface.

Table 2-1. **CPU Block Address Map**

Address	Description	Usage
0x0001_0000 – 0x0001_FFFF	USB Controller PIO Registers	USB Programmed Input Output
0x0005_0000 – 0x0005_0FFF	Reset/Clock Control Registers	Reset/Clock Control
0x0005_5000 – 0x0005_5FFF	USB Controller DMA Registers	USB Rx/Tx DMA Control
0x0005_B000 – 0x0005_BFFF	SPI Control Registers	Serial Peripheral Interface Control

2.1.3 Serial EEPROM Interface

The AR9281 provides a serial interface to access an external EEPROM. The EEPROM interface modifies configuration space registers and configuration- and vendor-specific information.

The off-chip EEPROM can be:

- A 4-Kb device, organized as 256 entries of 16 bits each (256x16)

The hardware automatically detects the EEPROM size. The EEPROM addressing is 16 bits wide, with each 16-bit EEPROM mapped into the AR9281's register space. Each 32-bit aligned address corresponds to a unique EEPROM location. Because the host interface supports 32-bit register accesses and ignores the two least significant address bits, the address offset provided by the host interface corresponds to four times the EEPROM location.

At reset, some USB configuration registers load from the EEPROM while others are programmed by the host or initialized by AR9281 hardware. To ensure that the EEPROM contents are valid, a 16-bit word at address offset 0x2000 is checked. If the values do not match 0xA55A, the EEPROM contents are ignored and the default values loaded. More information is provided in "Host Interface Registers" on page 93.

2.1.4 EEPROM Auto-Sizing Mechanism

The first procedure after reset is to read the offset address 0x2000 to check for the content 0xA55A. The EEPROM physical presence, programmed state, and size are determined automatically. If the offset address 0x2000 contents do not match the 0xA55A value for any supported EEPROM sizes, the AR9281 assumes the EEPROM is not present on the PCB, or is present but not programmed. In either case, the logic uses the default values as described in "Serial EEPROM Interface".

2.1.5 EEPROM Read/Write Protection Mechanism

The EEPROM contains a 16-bit word protect mask value at address location 0x2010 that prevents software from accessing certain regions. The mask is 16 bits wide and contains eight sub-masks that are 2 bits wide.

The sub-mask can have four values that determine the access types permitted to the associated protection region:

- 00: Read/write access allowed
- 01: Write-only access allowed
- 10: Read-only access allowed
- 11: No access allowed

2.2 Reset

The RST_L pin controls the AR9281 chip reset. The AR9281 host interface receives one reset signal as below:

- RST_L pin
  Controls the AR9281 power reset

In addition, the RTC_RESET register provides software control of warm reset for the MAC/baseband and PCU blocks. See the register "RTC Reset and Force Sleep and Force Wakeup (RTC_RESET)" on page 105.

2.3 GPIO

The AR9281 provides sixteen configurable bi-directional general purpose I/O ports. Each GPIO can be independently configured as input or output using the GPIO control register. Information presented at the GPIO inputs and outputs can be read from the register H_GPIO_IN_OUT (see "GPIO Input and Output (H_GPIO_IN_OUT)" on page 98).

2.4 LED

The AR9281 provides GPIO pins to configure for LED output. Control for LED output is provided by the MAC_LED register (see "MAC Interface Registers" on page 108).

2.5 USB Host Interface

This section provides a summary of the AR9281 USB interface. This interface is compliant with the USB 2.0 standard. It functions as the host interface for the AR9281, providing data and command transfer between the host software, the MAC, and the configuration registers. For details, refer to the USB 2.0 standards specifications.

2.6 The CPU Block

The CPU Block includes five major parts: CPU, Memory Controller, AHB Arbiter, the internal memory and the AHB process. The CPU Block controls the data path from the host to the WLAN and vice versa. The CPU Block also includes controlling the external SPI flash. See Figure 2-2 for a visual description of the CPU block.

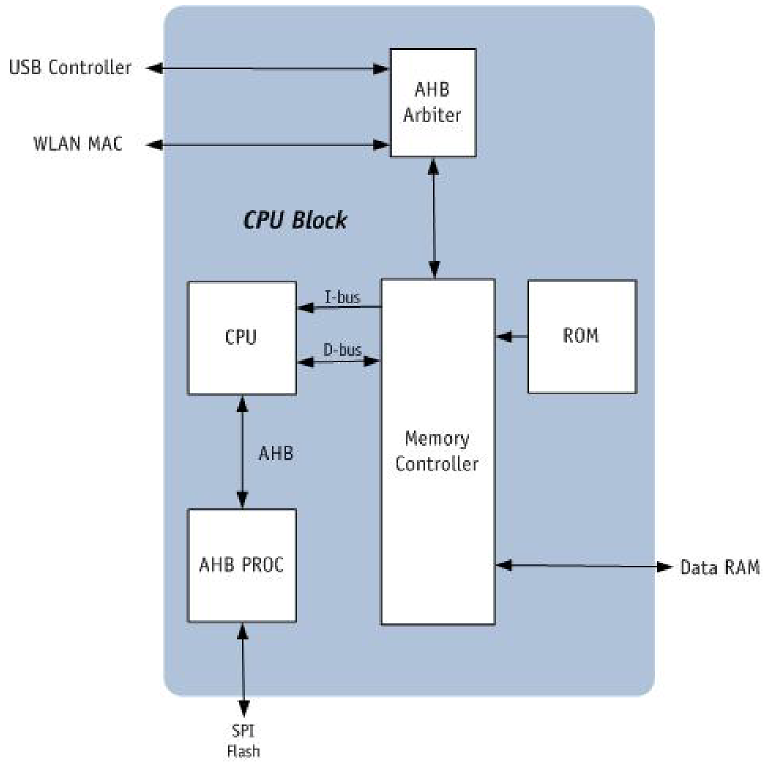


Figure 2-2. **CPU Block**

2.6.1 The CPU

The AR9271 uses an embedded CPU (117 MHz) which has three IO ports for data access. The I-bus is the channel used to get the program code from the ROM or the RAM. The D-bus is used to access data in the RAM. The AHB port provides the channel to access the SPI flash and controls access to the MAC registers.

2.6.2 Memory Controller and the AHB Arbiter

The Memory Controller module provides the channel for bus masters to access the memories within the AR9271. The internal ROM can be accessed by the CPU only, and the RAM can be accessed by the CPU, MAC DMA and the USB DMA. The AHB arbiter provides arbitration for these three masters. The Priority changes and determined by round-robin scheduling.

2.6.3 Internal Memories

The AR9271 has two internal memories, the ROM (24 KB) and the RAM (160 KB). The ROM provides the boot up sequence and various control mechanisms. The RAM is used to store part of the program code and all data packets for transmission and receiving.

2.6.4 The AHB Proc

The AHB Proc is a channel for the CPU to access the external flash. The CPU also accesses the MAC registers through the AHB Proc.

3. Medium Access Control (MAC)

The MAC consists of the following major functional blocks: 10 queue control units (QCUs), 10 distributed coordination function (DCF) control units (DCUs), a single DMA Rx unit (DRU), and a single protocol control unit (PCU). See Figure 3-1.

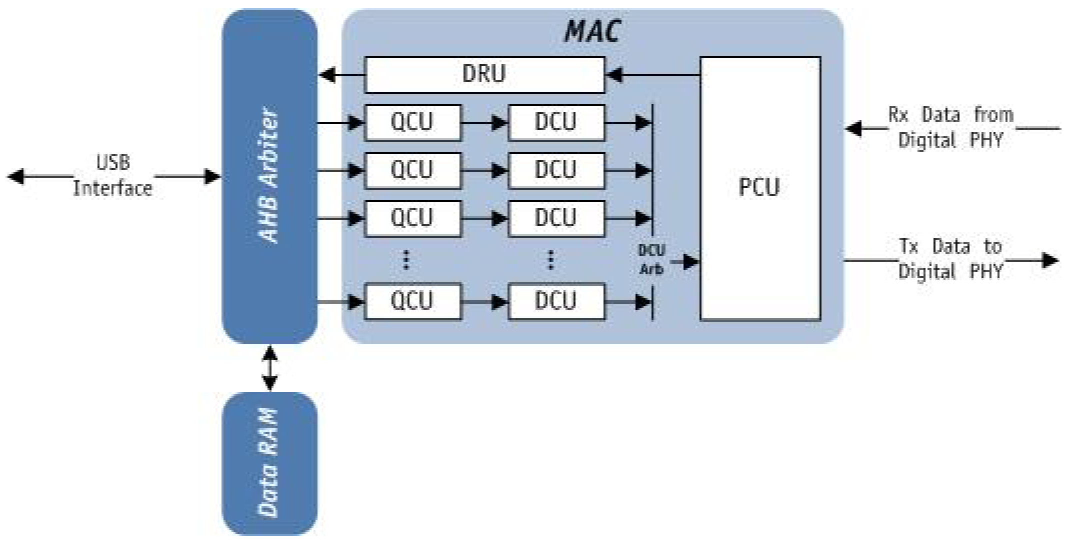


Figure 3-1. **MAC Block Diagram**

3.1 Overview

The MAC block supports full bus-mastering descriptor-based scatter/gather DMA. Frame transmission begins with the QCUs. QCUs manage the DMA of frame data from the host through the USB interface, and determine when a frame is available for transmission.

Each QCU targets exactly one DCU. Ready frames are passed from a QCU to its targeted DCU. The DCU manages the enhanced distributed coordination function (EDCF) channel access procedure on behalf of the QCUs associated with it.

Functionality of the MAC block includes:

- Tx frame data transfer from the host to the radio block using the USB interface
- Rx frame data transfer from the radio block to host using the USB interface
- Register access to all AR9281 registers
- Interrupt generation and reporting
- Sleep-mode (power-down) sequencing
- Miscellaneous error and status reporting functions

Once the DCU gains access to the channel, it passes the frame to the PCU, which encrypts the frame and sends it to the baseband logic. The PCU handles both processing responses to the transmitted frame, and reporting the transmission attempt results to the DCU.

Frame reception begins in the PCU, which receives the incoming frame bitstream from the digital PHY. The PCU decrypts the frame and passes it to the DRU, which manages Rx descriptors and writes the incoming frame data and status to the host memory through the USB interface.

3.2 Descriptor

The MAC is responsible for transferring frames between the host memory (accessed using the USB interface) and the AR9281. For all normal frame transmit/receive activity, the host provides a series of descriptors to the MAC, and the MAC then parses the descriptors and performs the required set of data transfers.

3.3 Descriptor Format

The transmit (Tx) descriptor format contains twenty-four 32-bit words and the receive (Rx) descriptor thirteen 32-bit words (see Table 3-1).

The first two words of the descriptor point to the next descriptor in the linked list and to the data buffer associated with the descriptor. Other words carry additional control information that affects how the MAC processes the frame and its data.

A descriptor is required to be aligned on a 32-bit boundary in host memory, although best performance is achieved if the descriptor is aligned on a cache-line boundary. The MAC uses the final two words to report status information back to the host. See:

Table	Description
Table 3-1	DMA descriptor format
Table 3-2	Tx control descriptor format (words 2–13)
Table 3-3	Tx status descriptors (words 14–23)
Table 3-4	Rx control descriptor (words 2–3)
Table 3-5	Rx status descriptor (words 4–12)

Table 3-1. **DMA Descriptor Format**

Word	Bits	Field Name	Description
0	31:0	link_ptr	Link pointer. Contains the address of the next descriptor to be used; must be 32-bit aligned (bits [1:0] must be 0)
1	31:0	buf_ptr	Data buffer pointer. Contains the starting address of the data buffer associated with this descriptor. A Tx data buffer can begin at any byte address. A Rx data buffer must be aligned on a 32-bit boundary in host memory, although best performance is achieved if the Rx data buffer is cache-line aligned. (Cache-line size varies from system to system.)
2–13 (Tx) 2–3 (Rx)	31:0	Host-to-DMA engine control information	Additional control information is passed from host to DMA engine. The format of these words varies depending on whether the descriptor is being used to Tx a frame from host to PCU, or Rx a frame from PCU to host. (See Table 3-2 on page 19, and Table 3-4 on page 29 for details.)
14–23 (Tx) 4–12 (Rx)	31:0	DMA completion status information	Status information reported by the DMA engine when it has finished processing a descriptor. As with the control information, the format of the status information differs between Tx and Rx descriptors. (See Table 3-3 on page 25, and Table 3-5 on page 29 for details.)

The Tx descriptor format for words 2 through 13 is described in Table 3-2.

Table 3-2. **Tx Control Descriptor Format (Words 2–13)**

Word	Bits	Field Name	Description
2	11:0	frame_length	Frame length Specifies the length, in bytes, of the entire MAC frame, including the frame check sequence (FCS), initialization vector (IV), and integrity check value (ICV) fields.
	12	vmf	Virtual more fragment If this bit is set, bursting is enabled for this frame. If no burst is in progress, it initiates a CTS-protected burst if cts_enable is set. If a previous burst is in progress, it ignores the cts_enable bit and assumes the burst is protected.
	13	RES	Reserved
	14	low_rx_chain	When set to 1, indicates that the Rx chain mask switches to low power mode after transmitting this frame
	15	clear_retry	Setting this bit disables the retry bit from being set in the Tx header on a frame retry
	21:16	tpc_0	Tx power control for series 0 These bits pass unchanged to the baseband, where they are used to control the transmit power for the frame.
	22	rts_enable	Request to send (RTS) enable. At most, one of the "rts_enable" and "cts_enable" bits may be set; it is illegal to set both. set: PCU transmits the frame using the RTS/CTS protocol clear: PCU transmits the frame using the contention/backoff protocol
	23	veol	Virtual end-of-list flag When set, indicates that the QCU should act as though the descriptor had a NULL LinkPtr, even if the LinkPtr is not NULL. Must be valid in the final descriptor of a frame and must be clear for all other descriptors of the frame.
	24	clear_dest_mask	Clear destination mask bit flag If set, instructs the PCU and DCU to clear the destination mask bit at the index specified by the DestIdx field.
	28:25	RES	Reserved
	29	int_req	Interrupt request flag Set to one by the driver to request that the DMA engine generate an interrupt upon completion of the frame to which this descriptor belongs. Note that this field must be valid and identical for all descriptors of the frame; that is, all descriptors for the frame must have this flag set, or all descriptors for the frame must have this flag clear.
	30	dest_index_valid	Destination index valid flag Specifies whether the contents of the DestIdx field are valid.
	31	cts_enable	Proceed frame with CTS flag If set, the PCU first sends a CTS before sending the frame described by the descriptor. Used for 802.11g and Atheros XR frames to quiet legacy stations before sending a frame the legacy stations cannot interpret (even at the PHY level). At most, one of the "rts_enable" and "cts_enable" bits may be set; it is illegal to set both bits.

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description	
3	11:0	buf_len	Data buffer length Specifies the length, in bytes, of the data buffer associated with this descriptor. Tx data buffers may be any non-zero length buffers. This field must be valid for all descriptors.	
	12	more	More descriptors in this frame flag Set to one by the driver to indicate additional descriptors (DMA fragments) exist in the current frame. This field must be valid for all descriptors.	
			0	No more descriptors for the current frame
			1	The current frame is continued in the next descriptor
	19:13	dest_index	Destination table index Specifies an index to an on-chip table of per-destination information. The PCU fetches the encryption key from the specified index in this table and uses the key to encrypt the frame. DMA logic uses the index to maintain per-destination Tx filtering status and other related information.	
	23:20	frame_type	Frame type indication Indicates to the PCU what type of frame is being sent. Supported values:	
			0	Normal frame
			1	Announcement traffic indication message (ATIM) frame
			2	PS poll frame
			3	Beacon
			4	Probe response frame
			15:5	Reserved
	24	no_ack	No ACK flag Must be set for any frame that has the 802.11 NoAck bit set in the QoS field and for all other frame types (e.g., beacons) that do not receive ACKs.	
			1	Do not wait for ACK
	28:25	RES	Reserved	
	29	more _agg	Indicates aggregate boundaries	
	30	is_agg	Set for all descriptors for an aggregate	
	31	more_rifs	More RIFS burst flag. When set, indicates that the current packet is not the last packet of an aggregate. All descriptors for all packets of an RIFS burst except the descriptors of the last packet must have this bit set. All descriptors of the last packet of an RIFS burst must have this bit as clear.	

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description
4	14:0	burst_duration	Burst duration value (in µs) If this frame is not part of a burst or the last frame in a burst, the value should be zero. In a burst, the value is the amount of time to reserve (via NAV) after completing the current Tx packet sequence (after the ACK if applicable).
	15	dur_update_en	Frame duration update control If set, the MAC updates (overwrites) the duration field in the frame based on the current Tx rate. If clear, the MAC does not alter the contents of the frame's Duration field. Note that the MAC changes only the frame's Duration field. It does not alter the Duration field in the RTS/CTS that precedes the frame itself if "rts_enable" or "cts_enable" is set.
	19:16	tx_tries0	Number of frame data exchange attempts permitted for Tx series 0 A "frame data exchange attempt" means a transmission attempt in which the actual frame is sent on the air (in contrast to the case in which the frame has RTS enabled and the RTS fails to receive a CTS). In this case, the actual frame is not sent on the air, so this does not count as a frame data exchange attempt. A value of zero is illegal for the TXDataTries0 field.
	23:20	tx_tries1	Number of frame data exchange attempts permitted for transmission series 1. A value of zero means skip this transmission series.
	27:24	tx_tries2	Number of frame data exchange attempts permitted for transmission series 2. A value of zero means skip this transmission series.
	31:28	tx_tries3	Number of frame data exchange attempts permitted for transmission series 3. A value of zero means skip this transmission series.

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description
5	7:0	tx_rate0	Tx rate for transmission series 0.

Rate	Desc	Rate	Desc
0x1–0x7	RES	0x18	CCK_11Mb_L
0x8	OFDM_48Mb	0x19	CCK_5_5Mb_L
0x9	OFDM_24Mb	0x1A	CCK_2Mb_L
0xA	OFDM_12Mb	0x1B	CCK_1Mb_L
0xB	OFDM_6Mb	0x1C	CCK_11Mb_S
0xC	OFDM_54Mb	0x1D	CCK_5_5Mb_S
0xD	OFDM_36Mb	0x1E	CCK_2Mb_S
0xE	OFDM_18Mb		
0xF	OFDM_9Mb		

Rate [1]	Desc	Stream	HT20 GI = 0 (Mbps)	HT40 GI = 0 (Mbps)	HT20 GI = 1 (Mbps)	HT40 GI = 1 (Mbps)
0x80	MCS 0	1	6.5	13.5	7.2	15
0x81	MCS 1	1	13	27	14.4	30
0x82	MCS 2	1	19.5	40.5	21.7	45
0x83	MCS 3	1	26	54	28.9	60
0x84	MCS 4	1	39	81	43.3	90
0x85	MCS 5	1	52	108	57.8	120
0x86	MCS 6	1	58.8	121.5	65.0	135
0x87	MCS 7	1	65	135	72.2	150

[1]All rates listed that are not listed here are reserved

Word	Bits	Field Name	Description
	15:8	tx_rate1	Tx rate for transmission series 1. See the rate table in "tx_rate0".
	23:16	tx_rate2	Tx rate for transmission series 2. See the rate table in "tx_rate0".
	31:24	tx_rate3	Tx rate for transmission series 3. See the rate table in "tx_rate0".
6	14:0	packet_duration0	Packet duration 0 (in µs) Duration of the actual Tx frame associated with TXRate0. This time does not include RTS, CTS, ACK, or any associated SIFS.
	15	rts_cts_qual0	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 0. 1 Default behavior with respect to "rts_enable" and "cts_enable"
	30:16	packet_duration1	Packet duration 1 (in µs) Duration of the actual Tx frame associated with TXRate1. This time does not include RTS, CTS, ACK, or any associated SIFS.
	31	rts_cts_qual1	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 1. 1 Default behavior with respect to "rts_enable" and "cts_enable"

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description		
7	14:0	packet_duration2	Packet duration 2 (in µs) Duration of the actual Tx frame associated with TXRate2. This time does not include RTS, CTS, ACK, or any associated SIFS.		
	15	rts_cts_qual2	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 2.		
			1	Default behavior with respect to"rts_enable" and "cts_enable"	
	30:16	packet_duration3	Packet duration 3 (in µs) Duration of the actual Tx frame associated with TXRate3. This time does not include RTS, CTS, ACK, or any associated SIFS.		
	31	rts_cts_qual3	Qualifies "rts_enable" or "cts_enable" in the Tx descriptor for Tx series 3.		
			1	Default behavior with respect to "rts_enable" and "cts_enable"	
8	15:0	agg_length	Aggregate length		
	17:16	RES	Reserved		
	25:18	pad_delim	Number of delimiters to add at the end of a packet. The encryption field must be valid for all descriptions.		
	28:26	encrypt_type	Encryption type		
			0	None	0 pad bytes
			1	WEP	4 pad bytes
			2	AES	8 pad bytes
			3	TKIP	12 pad bytes
	31:29	RES	Reserved		

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description	
9	0	20_40_0	20_40 control for Tx series 0	
			0	HT20 Tx Packet
			1	HT40 Tx packet
	1	GI_0	Guard interval control for Tx series 0	
			0	Normal guard interval
			1	Short guard interval
	4:2	chain_sel_0	Chain select for Tx series 0.	
			Bit [0]	Chain 0 is active
			Bit [1]	Reserved
			Bit [2]	Reserved
	5	20_40_1	20_40 control for Tx series 1	
			0	HT20 Tx Packet
			1	HT40 Tx packet
	6	GI_1	Guard interval control for Tx series 1	
			0	Normal guard interval
			1	Short guard interval
	9:7	chain_sel_1	Chain select for Tx series 1.	
			Bit [0]	Chain 0 is active
			Bit [1]	Reserved
			Bit [2]	Reserved
	10	20_40_2	20_40 control for Tx series 2	
			0	HT20 Tx Packet
			1	HT40 Tx packet
	11	GI_2	Guard interval control for Tx series 2	
			0	Normal guard interval
			1	Short guard interval
	14:12	chain_sel_2	Chain select for Tx series 2.	
			Bit [0]	Chain 0 is active
			Bit [1]	Reserved
			Bit [2]	Reserved
	15	20_40_3	20_40 control for Tx series 3	
			0	HT20 Tx Packet
			1	HT40 Tx packet
	16	GI_3	Guard interval control for Tx series 3	
			0	Normal guard interval
			1	Short guard interval
	19:17	chain_sel_3	Chain select for Tx series 3.	
			Bit [0]	Chain 0 is active
			Bit [1]	Reserved
			Bit [2]	Reserved
	27:20	rts_cts_rate	RTS or self-CTS rate selection Specifies the rate at which the RTS will send if "rts_enable" is set, or at which self CTS will send if cts_enable is set. See the rate table in "tx_rate0".	
	31:28	RES	Reserved	

Table 3-2. **Tx Control Descriptor Format (Words 2–13) (continued)**

Word	Bits	Field Name	Description
10	23:0	antenna_0	Antenna switch for Tx series 0
	31:24	RES	Reserved
11	23:0	antenna_1	Antenna switch for Tx series 1
	29:24	tpc_1	Tx power control (TPC) for Tx series 1 These bits pass unchanged to the baseband to control Tx power for the frame.
	31:30	RES	Reserved
12	23:0	antenna_2	Antenna switch for Tx series 2
	29:24	tpc_2	Tx power control (TPC) for Tx series 2 These bits pass unchanged to the baseband to control Tx power for the frame.
	31:30	RES	Reserved
13	23:0	antenna_3	Antenna switch for Tx series 3
	29:24	tpc_3	Tx power control (TPC) for Tx series 3 These bits pass unchanged to the baseband to control Tx power for the frame.
	31:30	RES	Reserved

The Tx descriptor format for words 14 through 24 is described in Table 3-3.

Table 3-3. **Tx Status Descriptor Format (Words 14–23)**

Word	Bits	Field Name	Description
14	7:0	rssi_ant00	Rx ACK signal strength indicator of control channel chain 0. A value of 0x80 (–128) indicates an invalid number.
	29:8	RES	Reserved
	30	ba_status	Block ACK status. If set, this bit indicates that the ba_bitmap values are valid
	31	RES	Reserved

Table 3-3. **Tx Status Descriptor Format (Words 14–23) (continued)**

Word	Bits	Field Name	Description
15	0	frm_xmit_ok	Frame transmission success set: The frame was transmitted successfully clear: No ACK or BA was received during frame transmission
	1	excessive_retries	Excessive tries If set, transmission of the frame failed because the try limit was reached before the frame was transmitted successfully. Valid only for the final descriptor of a frame, and only if "frm_xmit_ok" is clear.
	2	fifo_underrun	Tx FIFO underrun flag If set, frame transmission failed because the DMA engine was not able to supply the PCU with data as quickly as the baseband was requesting data. Valid for only non-aggregate or non-RIFS underrun conditions unless the underrun occurred on the first packet of the aggregate or if there was an RIFS burst. See also the description for "tx_dlmtr_ underrun_err" and "tx_data_ underrun_err". Valid only if "frm_xmit_ok" is clear.
	3	filtered	Frame transmission filter indication If set, indicates that frame was not transmitted because the corresponding destination mask bit was set when the frame reached the PCU, or the frame violated TXOP on the first packet of a burst. Valid if "frm_xmit_ok" is clear.
	7:4	rts_fail_cnt	RTS failure count Reports the number of times an RTS was sent but no CTS was received for the final transmission series (see "final_tx_index"). For frames with "rts_enable" clear, this count is always zero. Note that this count increments only when the RTS/CTS exchange fails. In particular, this count does not increment if the RTS/CTS exchange succeeds but the frame itself fails because no ACK was received. Valid only for the final descriptor of a frame, regardless of the state of "frm_xmit_ok".
	11:8	data_fail_cnt	Data failure count Reports the number of times the actual frame (as opposed to the RTS) was sent but no ACK was received for the final transmission series (see "final_tx_index"). Valid only for the final descriptor of a frame, regardless of the state of "frm_xmit_ok".
	15:12	virtual_retry_cnt	Virtual collision count Reports the number of virtual collisions that occurred before transmission of the frame ended. The counter value saturates at 0xF. A virtual collision refers to the case, as described in the 802.11e QoS specification, in which two or more output queues contend for a TXOP simultaneously. In such cases, all lower-priority output queues experience a "virtual collision" in which the frame is treated as if it had been sent on the air but failed to receive an ACK.
	16	tx_dlmtr_ underrun_err	Tx delimiter underrun error. This error only occurs on aggregate frames when the underrun conditions happen while the MAC is sending delimiters
	17	tx_data_ underrun_err	Tx data underrun error This error only occurs on aggregate frames when the underrun conditions happen while the MAC is sending the adata portion of the frame or delimiters
	18	desc_config_error	This error occurs if the current 20_40 values are not among the four valid combinations, or if "tx_dlmtr_ underrun_err" or "tx_data_ underrun_err" are set.
	19	tx_timer_expired	Tx timer expired. This bit is set when the Tx frame takes longer to send to the baseband than is allowed based on the TX_TIMER register. Some regulatory domains require that Tx packets may not exceed a certain amount of transmit time.
	31:20	RES	Reserved

Table 3-3. **Tx Status Descriptor Format (Words 14–23) (continued)**

Word	Bits	Field Name	Description
16	31:0	send_timestamp	Timestamp at the start of transmit. A snapshot of the lower 32 bits of PCU's timestamp (TSF value). This field can aid the software driver in implementing requirements associated with the aMaxTransmitMSDULifetime MAC attribute. The Tx timestamp is sampled upon tx_frame signal rising that goes from the MAC to the baseband. This value corresponds to the last attempt at packet transmission (not the first attempt).
17	31:0	ba_bitmap_0-31	Block ACK bitmap 0 to 31. The values from the block that ACK received after successful transmission of an aggregate frame. Bit 0, if set, represents the successful reception of the packet with the sequence number matching the seq_num value.
18	31:0	ba_bitmap_32-63	Block ACK bitmap 32 to 63. The values from the block that ACK received after successful transmission of an aggregate frame. Bit 0, if set, represents the successful reception of the packet with the sequence number matching the seq_num + 32.
19	7:0	rssi_ant10	Receive ACK signal strength indicator of the combination of all active chains on the control and extension channels. The value of 0x80 (-128) is used to indicate an invalid number.
	23:8	RES	Reserved
	31:24	ack_rssi_combined	Receive ACK signal strength indicator of combination of all active chains on the control and extension channels. The value of 0x80 (–128) is used to indicate an invalid number.
20	31:0	EVM	Error vector magnitude 0. EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.
21	31:0	EVM	Error vector magnitude 1. EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.
22	31:0	EVM	Error vector magnitude 2. EVM is not calculated for legacy frames so this value should always be 0x80 because ACK/BA should be sent at legacy rates.

Table 3-3. **Tx Status Descriptor Format (Words 14–23) (continued)**

Word	Bits	Field Name	Description
23	0	done	Descriptor completion flag. Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information. Valid only for the final descriptor of a frame, regardless of the state of "frm_xmit_ok". The driver is responsible for tracking what descriptors are associated with a frame. When the DMA engine sets the Done flag in the final descriptor of a frame, the driver must be able to determine what other descriptors belong to the same frame and thus also have been consumed.
	12:1	SeqNum	Tx sequence number. Indicates the sequence number from the response block ACK. This field should only be consulted if the Tx frame was an aggregate. Because hardware does not update the sequence number, this field does not need to be consulted for aggregate frames. For aggregates, this sequence number may not be the sequence number of the first Tx frame of the aggregate. More than likely it contains an older sequence number if the hardware of the other side keeps track of prior sequence numbers. It may sometimes have a newer sequence number if the first number of the aggregate failed.
	16:13	RES	Reserved
	17	txop_exceeded	TXOP has been exceeded. Indicates that this Tx frame had to be filtered because the amount of time to transmit this packet sequence would exceed the TXOP limit (which should only occur when software programs the TXOP limit improperly).
	20:18	RES	Reserved
	22:21	final_tx_index	Final transmission attempt series index. Specifies the number of the Tx series that caused frame transmission to terminate.
	24:23	RES	Reserved
	25	pwr_mgmt	Power management state. Indicates the value of the power management bit in the frame control field of the response ACK frame.
	27:26	RES	Reserved
	31:28	tid	Traffic identifier of block ACK. This field indicates the TID of the response block ACk. This field is only valid on the last descriptor of the last packet of an aggregate.

The DMA Rx logic (the DRU block) manages Rx descriptors and transfers the incoming frame data and status to the host through the USB Interface. The Rx descriptor format for words 2 and 3 is described in Table 3-4.

Table 3-4. **Rx Control Descriptor Format (Words 2–3)**

Word	Bits	Field Name	Description
2	31:0	RES	Reserved
3	11:0	buf_len	Data buffer length (in bytes). Specifies the length of the data buffer associated with this descriptor. Rx data buffers must have a length that is an integral multiple of four bytes.
	12	RES	Reserved
	13	int_req	Interrupt request flag. Indicates whether the DMA engine should generate an interrupt upon frame completion. 0: Do not generate an InterReq interrupt upon frame completion 1: Generate an InterReq interrupt upon frame completion
	31:14	RES	Reserved

The Rx descriptor format for words 4 through 13 is described in Table 3-5.

Table 3-5. **Rx Status Descriptor Format (Words 4–12)**

Word	Bits	Field Name	Description
4	7:0	rssi_ant00	Receive signal strength indicator of control channel chain 0. A value of 0x80 (–128) indicates an invalid number.
	23:8	RES	Reserved
	31:24	rx_rate	Rx rate indication. Indicates the rate at which this frame transmits from the source. Encodings match those used for the tx_rate_* field in word 5 of the Tx descriptor. Valid only if "frame_rx_ok" is set, or if it is clear and the "phy_error" flag is clear.
5	11:0	data_len	Received data length Specifies the length, in bytes, of the data actually received into the data buffer associated with this descriptor. The actual received data length is between zero and the total size of the data buffer, as specified originally in this field (see the description for "buf_len"). Valid for all descriptors.
	12	more	More descriptors in this frame flag If set, then this is not the final descriptor of the frame. If clear, this descriptor is the final one of the frame. Valid for all descriptors. 0: No more descriptors for the current frame 1: The current frame is continued in the next descriptor
	13	RES	Reserved
	21:24	num_delim	Number of 0 length pad delimiters after the current packet. This field does not include the start delimiter required between each packet in an aggrgate. This field is only valid for aggregate packets, except for the last packet of an aggregate.
	31:22	RES	Reserved

Table 3-5. **Rx Status Descriptor Format (Words 4–12) (continued)**

Word	Bits	Field Name	Description
6	31:0	rcv_timestamp	A snapshot of the PCU's timestamp (TSF value) (in ms) Bits [31:0] of the PCU's 64-bit TSF. Intended for packet logging and packet sniffing. The timestamp is sampled on the rising edge of rx_clear, which goes from the baseband to the MAC.
7	0	gi	Rx packet guard interval. If this value is clear, the Rx frame was an HT 20 packet (20 MHz bandwidth). If this value is set, then the receive frame used a short guard interval.
	1	20_40	Rx packet 20 or 40 MHz bandwidth indicator. If this value is clear, the Rx frame was an HT20 packet (20 MHz bandwidth). If this value is set, then the receive frame was an HT40 packet (40 MHz bandwidth).
	2	duplicate	Rx packet duplicate indicator. If this value is set, the baseband has determined that this packet is a duplicate packet.
	3	stbc	Receive packet STBC indicator. If this value is set, then the baseband has received STBC frames as indicated in the HT_PLCP.
	7:4	RES	Reserved
	31:8	rx_antenna	Rx antenna value.
8	7:0	rssi_ant10	Receive signal strength indicator of control channel chain 0. A value of 0x80 (-128) indicates an invalid number.
	23:8	RES	Reserved
	31:24	rssi_combined	Rx signal strength indicator of combination The value of 0x80 (-128) is used to indicate an invalid number.
9	31:0	EVM	Rx packet error vector magnitude 0.
10	31:0	EVM	Rx packet error vector magnitude 1.
11	31:0	EVM	Rx packet error vector magnitude 2.
12	0	done	Descriptor completion flag Set to one by the DMA engine when it has finished processing the descriptor and has updated the status information.Valid for all descriptors. 0: The MAC has not finished processing the descriptor. Valid only for the final descriptor of a frame 1: The MAC has finished processing the descriptor and has updated the status information
	1	frame_rx_ok	Frame reception success flag If set, the frame was received successfully. If clear, an error occurred during frame reception. 0: An error occurred during frame reception 1: Frame received successfully
	2	crc_error	Cyclic redundancy code (CRC) error flag Valid only for the final descriptor of a frame, and only if the "frame_rx_ok" flag is clear. 0: Frame received without a CRC error 1: Reception of frame failed because of an incorrect CRC value
	3	decrypt_crc_err	Decryption CRC failure flag. Valid only for the final descriptor of a frame, and only if the FrmRcvOK flag is clear.

Atheros Communications, Inc. COMPANY CONFIDENTIAL

Table 3-5. **Rx Status Descriptor Format (Words 4–12) (continued)**

Word	Bits	Field Name	Description
12 (cont.)	4	phy_error	PHY error flag. If set, then reception of the frame failed because the PHY encountered an error. In this case, bits [15:8] of this word indicate the specific type of PHY error; see the baseband specification for details. Valid only if the 'frame_rx_ok' flag is clear.
	5	mic_error	Michael integrity check error flag. If set, then the frame's TKIP Michael integrity check value did not verify correctly. Valid only when all of the following are true: ■ The "frame_rx_ok" bit is clear ■ The frame was decrypted using TKIP ■ The frame is not a fragment
	6	pre_delim_crc_err	Demiliter CRC error detected before this current frame
	7	RES	Reserved
	8	key_idx_valid	■ If "frame_rx_ok" is set, then this field contains the decryption key table index valid flag. If set, indicates that the PCU successfully located the frame's source address in its on-chip key table and that the KeyIdx field reflects the table index at which the destination address was found. If clear, indicates that the PCU failed to locate the destination address in the key table and that the contents of KeyIdx field are undefined. ■ If "frame_rx_ok" is clear and the "phy_error" bit is set, then this field contains bit [0] of the PHY error code. In both cases, this field is valid only for the final descriptor of a frame.
	15:9	key_idx	■ If "frame_rx_ok" is set, then this field contains the decryption key table index. If the "key_idx_valid" is set, then this field specifies the index at which the PCU located the frame's destination address in its on-chip decryption table. If the "key_idx_valid" is clear, the value of the field is undefined. ■ If "frame_rx_ok" is clear and the "phy_error" bit is set, then this field contains bit [7:1] of the PHY error code.
	16	more_agg	More aggregate flag. This bit is set to 1 in all packets of an aggregate that has another packetof the current aggregate to follow. If clear, indicates that this packet is the last one of an aggregate.
	17	aggregate	Aggregate flag. If set, indicates that this packet is part of an aggregate.
	18	post_delim_crc_err	Delimiter CRC error detected after this current frame. Only occurs when the start delimiter of the last frame in an aggregate is bad.
	27:19	RES	Reserved
	28	hi_rx_chain	Setting this bit indicates that the Rx chain control is in high power mode
	29	first_agg	Indicates that this packet is the first one of an aggregate.
	30	decrypt_busy_err	Decrypt busy error. If set it indicates new frame arrived before decryption completed for the previous frame.
	31	key_miss	Key cache miss indication. If set, indicates that the PCU could not locate a valid description key for the frame. Valid only if the "frame_rx_ok" is clear.

3.4 Queue Control Unit (QCU)

The queue control unit performs two tasks:

- Managing the Tx descriptor chain processing for frames pushed to the QCU from the host by traversing the linked list of Tx descriptors and transferring frame data from the host to the targeted DCU.
- Managing the queue Tx policy to determine when the frame at the head of the queue should be marked as available to transmit.

The MAC contains ten QCUs, each with all the logic and state registers needed to manage a single queue (linked list) of Tx descriptors. A QCU is associated with exactly one DCU. When a QCU prepares a new frame, it signals ready to the DCU. When the DCU accepts the frame, the QCU responds by getting the frame data and passing it to the DCU for eventual transmission to the PCU and on to the air. The host controls how the QCU performs these tasks by writing to various QCU configuration registers (see "QCU Registers" on page 76).

3.4.1 DCF Control Unit (DCU)

Collectively, the ten DCUs implement the EDCF channel access arbitration mechanism defined in the Task Group E (TGe) QoS extension to the 802.11 specification. Each DCU is associated with one of the eight EDCF priority levels and arbitrates with the other DCUs on behalf of all QCUs associated with it. A central DCU arbiter monitors the state of all DCUs and grants one the next access to the PCU (that is, access to the channel).

Because the EDCF standard defines eight priority levels, the first eight DCUs (DCUs 0–7) map directly to the eight EDCF priority levels. The two additional DCUs handle beacons and beacon-gated frames for a total of ten DCUs.

The mapping of physical DCUs to absolute channel access priorities is fixed and cannot be altered by software:

The highest-priority DCU is DCU 9. Typically, this DCU is the one associated with beacons. The next highest priority DCU is DCU 8. Typically, this DCU is the one associated with beacon-gated frames. The remaining eight DCUs priority levels are filled with DCUs 7 through 0. Among these 8 DCUs, DCU 7 has highest priority, DCU 6 the next highest priority, and so on through DCU 0, which has the lowest priority. Typically, these DCUs are associated with EDCF priorities seven through zero, respectively.

3.5 Protocol Control Unit (PCU)

The PCU is responsible for the details of sending a frame to the baseband logic for transmission, for receiving frames from the baseband logic and passing the frame data to the DRU, including:

- Buffering Tx and Rx frames
- Encrypting and decrypting
- Generating ACK, RTS, and CTS frames
- Maintaining the timing synchronization function (TSF)
- Inserting and verifying FCS
- Generating virtual clear channel assessment (CCA)
- Updating and parsing beacons
- The PCU is primarily responsible for buffering outgoing and incoming frames and conducting medium access compatible with the IEEE 802.11 DCF protocol.

Figure 3-2 shows the PCU functional block diagram.

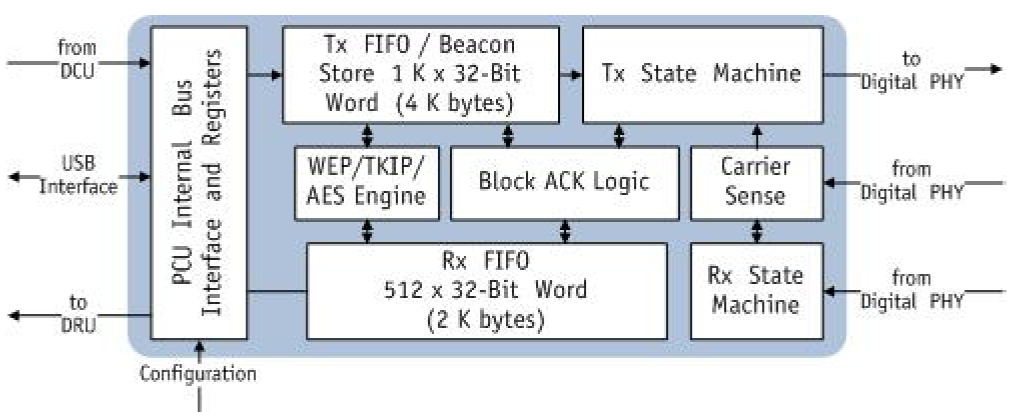


Figure 3-2. **PCU Functional Block Diagram**

4. Digital PHY Block

The digital physical layer (PHY) block is described in 802.11 draft-n mode and 802.11b/g legacy mode. Transmit and receive paths are provided and shown as block diagrams for 802.11 draft-n mode.

4.1 Overview

The digital PHY block is a half-duplex, OFDM, CCK, DSSS baseband processor compatible with IEEE 802.11n and 802.11b/g. The AR9281 supports PHY data rates up to 72.2 Mbps in 20- and 150 Mbps in 40-MHz channel modes and all data rates defined by the IEEE 802.11b/g standard (1–54Mbps). Modulation schemes include BPSK, QPSK, 16-QAM, 64-QAM and forward error correction coding with rates of 1/2, 2/3, 3/4, 5/6.

4.2 802.11n Mode

Frames beginning with training symbols are used for signal detection, automatic gain control, frequency offset estimation, symbol timing, and channel estimation. This process uses 56 sub-carriers for 20-MHz HT mode: 52 for data transmission and 4 for pilots. It uses 114 sub-carriers for 40-MHz HT mode: 108 for data transmission and 6 for pilots.

4.2.1 Transmitter (Tx)

Figure 4-1 shows the Tx path digital PHY 802.11n block diagram.

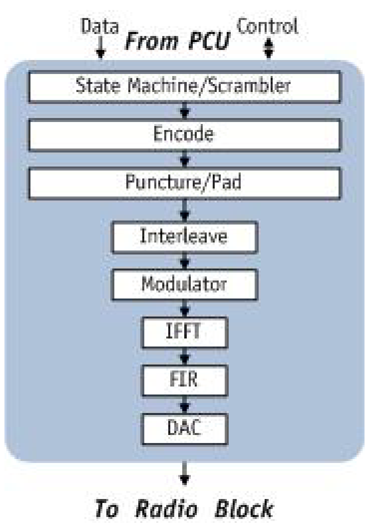


Figure 4-1. **Digital PHY 802.11n Tx**

The PCU block initiates transmission. The digital PHY powers on the digital to analog converter (DAC) and transmit portions of the AR9281. The training symbols are a fixed waveform and are generated within the digital PHY in parallel with the PCU sending the Tx header (frame length, data rate, etc.). The PCU must send transmitted data quickly enough to prevent buffers in the digital PHY from becoming empty. The PCU is prevented from sending data too quickly by pauses generated within the digital PHY.

Figure 4-1 shows a system with one spatial data stream. Puncturing and padding are added to the encoded data. At this point, it interleaves coded bits across different data subcarriers followed by the modulation, then the stream undergoes IFFT processing to produce time domain signals.

4.2.2 Receiver (Rx)

Figure 4-2 shows the Rx path digital PHY 802.11n block diagram.

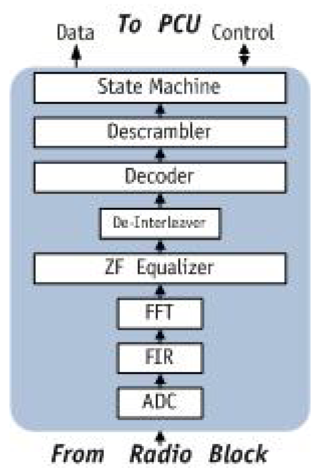


Figure 4-2. **Digital PHY 802.11n Rx**

The receiver inverts the transmitter's steps, performing a fast fourier transform (FFT), extracting bits from received constellations, de-interleaving, accounting for puncturing, decoding, and descrambling. The Rx block shows one spatial stream configuration. Figure 4-2 shows a frequency-domain equalizer handling degradation due to multi-path.

4.3 802.11b/g Legacy Mode

4.3.1 Transmitter

The AR9281 digital PHY incorporates an OFDM and DSSS transceiver that supports all data rates defined by IEEE 802.11b/g. Legacy mode is detected on per-frame basis. PLCP frames are detected for legacy network information. The transmitter switches dynamically to generate legacy signals.

4.3.2 Receiver

The receiver is capable of dynamically detecting legacy, HT 20 MHz or 40 MHz frames and will demodulate the frame according to the detected frame type.

5. Radio Block

The AR9271 consists of two LNAs, denoted as LNA1 and LNA2 in Figure 5-1. LNA2 is a dedicated Rx chain, while LNA1/Tx shares the Tx and Rx chains using an internal switch. Both LNA1 and LNA2 pass through an internal diversity combiner before being relayed on to the receiver. Four options exist for the combiner; LNA1, LNA2, LNA1-LNA2 and LNA1+LNA2. A software diversity algorithm determines which is used.

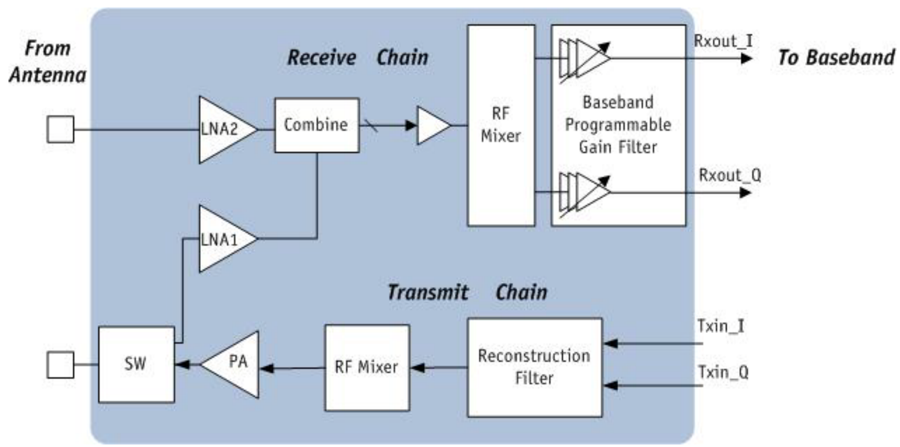


Figure 5-1. **Radio Functional Block Diagram**

5.1 Receiver (Rx) Block

The receiver converts an RF signal (with 20 MHz or 40 MHz bandwidth) to baseband I and Q outputs. The dual band receiver operates in the 2.4 GHz bands to support CCK and OFDM signals for 802.11b, 802.11g, and 802.11n.

The 2.4 GHz receiver implements a direct conversion architecture.

The receiver consists of low noise amplifiers (LNA1 and LNA2), diversity combiner in-phase (I) and quadrature (Q) radio frequency mixers, and a baseband programmable gain amplifier (PGA). The mixer converts the output of the on-chip LNA to baseband I and Q signals. The I and Q signals are low-pass filtered and amplified by a baseband programmable gain filter controlled by digital logic. The baseband signals are sent to the ADC within the MAC/Baseband processor.

The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/ Baseband processor. Additionally, the receive chain can be digitally powered down to conserve power.

5.2 Transmitter (Tx) Block

The transmitter converts baseband I and Q inputs to 2.4 GHz RF outputs as shown in Figure 5-1. The inputs to the transmitter are current outputs of the DAC within the MAC/ Baseband processor. These currents are low-pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

The I and Q signals are converted to RF signals using an integrated up-conversion architecture. The baseband I and Q signals are up-converted directly to RF using a pair of quadrature mixers. The internal power amplifier amplifies the signal power and then sends it to the antenna via an internal RF switch.

The transmit chain can be digitally powered down to conserve power. To ensure that the FCC limits are observed and the output power stays close to the maximum allowed, the transmit output power is adjusted by a closed loop, digitally programmed, control loop at the start of each packet. The ARXXXX provides a closed loop power control based on an on-chip power detector.

5.3 Synthesizer (SYNTH) Block

The radio supports one on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and transmitter mixers. The synthesizer has the topology shown in Figure 5-2.

The ARXXXX generates the reference input from a 40 MHz crystal for the synthesizer. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/frequency locked loop.

Upon power up or channel re-selection, the synthesizer takes approximately 0.2 ms to settle.

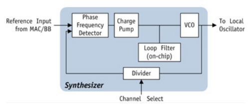


Figure 5-2. **Radio Synthesizer Block Diagram**

5.4 Bias/Control (BIAS) Block

The bias/control block provides the reference voltages and currents for all other circuit blocks (see Figure 5-3). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 KΩ ±1% resistor.

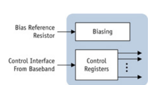


Figure 5-3. **Bias/Control Block Diagram**

6. Register Descriptions

This section describes the CPU Block registers and MAC registers for the various blocks of the AR9271. The AR9271 registers are mapped to the memory space of the internal CPU.

The AR9271 has two main register sections. One is the "CPU Block Register Summary" on page 37 which includes:

- "USB Controller PIO Registers" on page 37
- "Reset/Clock Control Register" on page 41
- "USB Controller DMA Registers" on page 48
- "SPI Control Registers" on page 54

The second register set is the "MAC Register Descriptions" on page 57 which includes:

- "General DMA and Rx-Related Registers" on page 57
- "QCU Registers" on page 76
- "DCU Registers" on page 83
- "Host Interface Registers" on page 93
- "RTC Interface Registers" on page 104
- "MAC Interface Registers" on page 108
- "MAC PCU Registers" on page 109

CPU Block

Table 6-1 summarizes the AR9271 CPU Block address space. At reset, an off-chip serialized EEPROM initializes some registers, while the CPU or the AR9271 hardware must program the others.

Table 6-1. **CPU Block Register Summary**

Address	Description	Page
0x0001_0000 – 0x0001_FFFF	USB Controller PIO Registers	page 37
0x0005_0000 – 0x0005_0FFF	Reset/Clock Control Registers	page 41
0x0005_5000 – 0x0005_5FFF	USB Controller DMA Registers	page 48
0x0005_B000 – 0x0005_BFFF	SPI Control Registers	page 54

6.1 USB Controller PIO Registers

This section describes the USB Controller PIO registers for the AR9271. Table 6-2 defines the address, type and page location of these registers.

Table 6-2. **USB Controller PIO Registers**

Address	Description	Page
0x0001_000C	Endpoint Data Port Register	page 38
0x0001_0100	USB Data Width Control Register	page 38
0x0001_0108	USB DMA Control Register	page 38
0x0001_0110	USB Upstream Stream Mode Max Aggregate Register	page 39
0x0001_0114	USB Upstream Mode Time Control Register	page 40
0x0001_0118	USB DMA Reset Control Register	page 40
0x0001_0120	USB Controller Wake Up	page 40
0x0001_0128	USB Clock Status Register	page 40

6.1.1 Endpoint Data Port Register (EP0_DB)

Address: 0x0001_000C
Access: Read/Write

This register is for Endpoint 0 data access.

Bit	Name	Type	Reset	Description
7:0	EP0_DB	R/W	0x0	Endpoint 0 Data Port Register for data access

6.1.2 USB Data Width Control Register (UC_CTL)

Address: 0x0001_0100
Access: Read/Write

This register identifies valid bytes in the data transfer from the C_BUS master to the EP0 data port.

Bit	Bit Name	Type	Reset	Description	
31:4	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
3:0	UC_BE	R/W	0xF	The signal UC_BE is used to indicate which bytes are valid in the data transfer from the C_BUS master to the EP0 data port. This is useful when transferring the last data of one packet. Each UC_BE bit represents C_BUS 8 bits, and all 1's should be conjunctive.	
				0001	Byte enabled
				0011	Word enabled
				0111	3 bytes enabled
				1111	Double word enabled (This will enable the double word except the last data of one packet)

6.1.3 USB DMA Control Register (UD_CTRL)

Address: 0x0001_0108
Access: Read/Write

This register defines the instances when the DMA should be enabled or disabled.

Bit	Bit Name	Type	Reset	Description	
31:11	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
10	MP_DS_ STREAM_ MODE	R/W	0x0	Used to enable or disable the medium priority stream mode.	
				0	Disable downstream stream mode
				1	Enable downstream stream mode
9	MP_DS_ DMA_EN (Host Out)	R/W	0x0	Medium priority downstream DMA enable. The DMA will start downstream data movement when it is idle. If the software needs to stop the DMA, this bit should be cleared and wait for the state machine to become idle.	
				0	Disable
				1	Enable
8	HP_DS_DMA_ EN (Host out)	R/W	0x0	High priority downstream DMA enable. The DMA will start downstream data movement when idle. If the software wishes to stop the DMA, this bit should to be cleared and then wait for the state machine to become idle.	
				0	Disable
				1	Enable
7	HP_DS_ STREAM_ MODE	R/W	0x0	Used to enable and disable the high priority downstream mode	
				0	Disable
				1	Enable

6	LP_DS_ STREAM_ MODE	R/W	0x0	Used to enable and disable the low priority downstream mode	
				0	Disable
				1	Enable
5:4	HOST_BUFFER _FIFO_SIZE	R/W	0x0	Defines the host buffer size. Used for stream mode. If the DMA counter reaches the size defined below, the DMA will send a zero packet to the host before the next data block.	
				00	4096 bytes
				01	8192 bytes
				10	16384 bytes
				11	32768 bytes
3	PACKET_ MODE	R/W	0x0	The USB upstream DMA can operate in either packet mode or stream mode. This bit must be set before the DMA is enabled.	
				0	Stream mode
				1	Packet mode
2	USB_SPEED_ IND	R/W	0x0	The CPU uses this bit to tell the DMA in which speed mode the USB is configured.	
				0	full speed
				1	high speed
1	US_DMA_EN (Host In)	R/W	0x0	Upstream DMA enable	
				0	Disable
				1	Enable
0	LP_DS_DMA_ EN (Host out)	R/W	0x0	Low priority downstream DMA enable. The DMA will start downstream data movement when it is idle. If the software wishes to stop DMA, this bit should be cleared and then wait for the state machine to become idle.	
				0	Disable
				1	Enable

6.1.4 USB Upstream Stream Mode MAX Aggregate Register (REG_APKT)

Address: 0x0001_0110
Access: Read/Write

This register is used to set the USB upstream mode's max aggregate packet setting.

Bit	Bit Name	Type	Reset	Description
31:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	USBUP_MAX_ PKTS_R	R/W	0x0	The USB upstream mode max aggregate setting. When the USB upload stream is enabled, the DMA will aggregate upstream packets to this register's setting in one USB transfer. Then the DMA will terminate the current USB transfer and start the next new transfer. A reading of 0 is one packet, a reading of 1 will aggregate 2 packet, a reading of 2 will aggregate 3 packets and so on until the number reaches 255, which aggregates 256 packets.

6.1.5 USB Upload Time Control

Address: 0x0001_0114

Access: Read/Write

This register defines the upload timeout count when in streaming mode.

Bit	Bit Name	Type	Reset	Description
31:12	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.
11:0	UP_TIME_CNTL	R/W	0x0	The upload timeout count for the stream mode. The USB will terminate the transfer if a time out occurs and no packet is received since the last received packet. The unit is measured in 32 USB clock (30 MHz) cycles.

6.1.6 USB DMA Reset Control Register

Address: 0x0001_0118

Access: Read/Write

This register is used to protect the DMA during a reset from the USB controller.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	DIS_USBRST	R/W	0x1	When this bit is set, the reset from the USB controller will not affect the DMA

6.1.7 USB Controller Wake Up

Address: 0x0001_0120
Access: Read/Write

This register is used to configure the settings for the power saving feature of the USB.

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.
1	PWR_SAV	R	0x0	Power saving indicator from the USB controller
0	WAKE	R/W	0x0	Remote wake-up to USB controller

6.1.8 USB Clock Status Register (US_CLK_STS)

Address: 0x0001_0128
Access: Read/Write

This register is used to configure the settling time of the USB controller's clock and to indicate the status of the clock's stability.

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.
8	USBCLK_STABLE	R/W	0x0	Indicates if the cycle count reaches the defined number in bit 7:0
7:0	CLK_STABLE_CNT	R/W	0x64	This bit defines the cycle count for USB clock to be stable

6.2 Reset/Clock Control Register

This section describes the Reset Clock Control registers for the AR9271. Table 6-3 defines the offset, type and page location of these registers.

Table 6-3. **Reset/Clock Control Registers**

Offset	Description	Page
0x0005_0000	General Purpose Timer Register	page 41
0x0005_0004	General Purpose Timer Reload Register	page 41
0x0005_0008	Watchdog Timer Control Register	page 42
0x0005_000C	Watchdog Timer Register	page 42
0x0005_0010	Reset Register	page 42
0x0005_0014	Bootstrap Values	page 42
0x0005_001C	Watchdog Timer Interrupt	page 43
0x0005_0020	General Timer Interrupt	page 43
0x0005_0040	Clock Control Register	page 43
0x0005_0044	Reset and Power Down Control Register	page 44
0x0005_0048	USB PLL Parameter Register	page 46
0x0005_004C	Reset Status Register	page 47
0x0005_0090	Chip Revision ID	page 47

6.2.1 General Purpose Timer Register (RST_GENERAL_TIMER)

Address: 0x0005_0000
Access: Read/Write

This register is a timer that counts down to zero, sets an interrupt, and then reloads from the General Timer Reload Register.

Bit	Bit Name	Type	Reset	Description
31:0	TIMER	R/W	0x0	Timer value.

6.2.2 General Purpose Timer Reload Register (RST_GENERAL_TIMER_RELOAD)

Address: 0x0005_0004
Access: Read/Write

This register contains the value that will be loaded into the General Purpose Timer register when it decrements to zero.

Bit	Bit Name	Type	Reset	Description
31:0	RELOAD_ VALUE	R/W	0x0	Timer reload value

6.2.3 Watchdog Timer Control Register (RST_WATCHDOG_TIMER_CONTROL)

Address: 0x0005_0008
Access: Read/Write

This register sets the action to take when the Watchdog Timer reaches zero. There are three options for the action: Non-maskable Interrupt and General Purpose Interrupt and Full-chip reset.

Bit	Bit Name	Type	Reset	Description	
31	LAST	R	0x0	Indicates if the last reset was due to a watchdog timeout.	
30:2	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.	
1:0	ACTION	R/W	0x0	Indicates the action to be taken after the Watchdog timer reaches zero.	
				00	No action
				01	General Purpose Interrupt
				10	NMI
				11	Full chip reset

6.2.4 Watchdog Timer Register (RST_WATCHDOG_TIMER)

Address: 0x0005_000C
Access: Read/Write

This register counts down to zero and when it reaches zero, performs the action specified in the Watchdog Timer Control register.

Bit	Bit Name	Type	Reset	Description
31:0	Timer	R/W	0x0	Counts down to zero and stays at zero until set to another value by software. This field should be set to a non-zero value before updating the Watchdog Timer Control register to a non-zero value.

6.2.5 Reset Register (RST_RESET)

Address: 0x0005_0010
Access: Read/Write

This register individually controls the reset to each of the chip's sub-modules.

Bit	Bit Name	Type	Reset	Description
31:22	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.
21	CPU_NMI	R/W	0x0	Sends an NMI to the CPU. Always zero when read.
20:0	RES	R	0	Reserved. Must be written with zero. Contains zeros when read.

6.2.6 Bootstrap Values (RST_BOOTSTRAP)

Address: 0x0005_0014
Access: Read-Only

This register contains the bootstrap values recorded during reset.

Bit	Bit Name	Type	Reset	Description
31:6	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
5	EEP_BUSY	R	0x0	Denotes that the EEPROM is busy

4	JTAG_SEL	R	0x0	If set, denotes the CPU JTAG interface. Otherwise, it is a normal JTAG interface.
3:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	EXT_BOOT	R	0x0	Used to denote where the chip boots. 0 — Boot from the internal EEPROM 1 — Boot from the external SPI Flash

6.2.7 Watchdog Timer Interrupt (RST_WATCHDOG_INT)

Address: 0x0005_001C
Access: Read-Only

This register contains the interrupt status of the watchdog timer.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	WATCHDOG_INT	R	0x0	Indicates the watchdog timer has expired

6.2.8 General Timer Interrupt (RST_GENERAL_TIMER_INT)

Address: 0x0005_0004
Access: Read-Only

This register indicates that the general timer has expired.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	GTMR_INT	R	0x0	Indicates the general timer has expired

6.2.9 Clock Control Register

Address: 0x0005_0040
Access: Read/Write

This register is used to configure the clock settings for the AR9271.

Bit	Bit Name	Type	Reset	Description
31:14	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
13:12	AHB_DIVIDE	R/W	0x0	AHB clock frequency division ratio (AHB Clock/CPU Clock) 00 — 1/1 01 — 1/2 10 — 1/4
11:9	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	SPI_SEL	R/W	0x0	Used to switch the function of I/O pins 18-21 between GPIO and SPI 0 — Sets the pins as GPIO 5-8 1 — Sets the pins as SPI
7:5	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.

Bit	Bit Name	Type	Reset	Description	
4	AHB_GATED	R/W	0x0	Used to set the AHB clock	
				0	Free running AHB clock
				1	AHB clock is gated
3	USB_CTL_CLK_ GATED	R/W	0x0	Used to enable or disable the USB controller clock	
				0	Keep USB controller clock running
				1	Gated USB controller clock
2:0	CPU_CLK	R/W	0x0	CPU clock selection	
				000	22 MHz
				001	88 MHz
				010	44 MHz
				101	117 MHz
				110	OSC 40 MHz

The AHB field in the previous register mentions the division ratio between the AHB clock and the CPU clock. The following table better defines this ratio in terms of MHz.

CPU Clock Rate (MHz)	AHB Clock Rate (MHz)		
	Ratio=1	Ratio=1/2	Ratio=1/4
117	117	117	117
88	88	44	22
44	44	22	11
22	22	11	5.5
40	40	40	40

6.2.10 Reset and Power Down Control Register

Address: 0x0005_0044
Access: Read/Write

This register is used to set the bits for power down and reset of the AR9271.

Bit	Bit Name	Type	Reset	Description	
31:21	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
20	GLBL_CLK_EN	R/W	0x0	Used to set the GLOBAL_CLK_EN	
				0	Sets the GLOBAL_CLK_EN to high
				1	Allows the MAC control the GLOBAL_CLK_EN of the radio
19	USB_PLL_PWD _CTL	R/W	0x0	Sets the type of mechanism to be used to power down the USB PLL	
				0	Allows the USB suspend mechanism to control the power down of the USB PLL
				1	Power down the USB PLL

18	MAIN_PLL_ PWD_CTL	R/W	0x0	Sets the type of mechanism to be used to power down the main PLL	
				0	Allows the USB suspend mechanism to control the power down of the main PLL
				1	Power down the main PLL
17	CLKIN_CTL	R/W	0x0	Sets the type of gate 40 MHz clock	
				0	Allows the USB suspend mechanism control the gate 40 MHz clock
				1	Gate 40 MHz clock
16:15	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.	
14	GATE_MAC_ CTL	R/W	0x0	Used to set the gate reset controls for the MAC	
				0	Gates the reset controls from the MAC
				1	Do not gate the reset controls from the MAC
13	USB_RST_SEL	R/W	0x0	Selects the source of the reset to the USB PHY	
				0	Determined by bit [12] (USB_POR)
				1	Uses the reset from the USB controller
12	USB_POR	R/W	0x0	The software controlled reset to the USB PHY	
				0	Deassert reset
				1	Assert reset
11	USB_SUSPEND	R/W	0x0	Used to configure suspension of the USB PHY	
				0	Allows the USB controller to control the suspend signal to the USB PHY
				1	Forces the suspend signal of the USB PHY to be 0, in suspend mode
10	BB_WARM_RST	R/W	0x0	The software controlled warm reset to the baseband	
				0	Deassert reset
				1	Assert reset
9	BB_COLD_RST	R/W	0x0	The software controlled cold reset to the baseband	
				0	Deassert reset
				1	Assert reset
8	CG_COLD_RST	R/W	0x0	The software controlled cold reset to clock generation and miscellaneous logic	
				0	Deassert reset
				1	Assert reset
7	RADIO_WARM _RST	R/W	0x0	The software controlled warm reset to radio	
				0	Deassert reset
				1	Assert reset
6	RADIO_COLD_ RST	R/W	0x0	The software controlled cold reset to radio	
				0	Deassert reset
				1	Assert reset

5	RADIO_RF_RST	R/W	0x1	The software controlled RF reset to radio	
				0	Deassert reset
				1	Assert reset
4	AHB_RST_MSK	R/W	0x0	Used to specify the AHB bus reset mask	
				0	The AHB bus will not be reset when bit [0] is set to 1
				1	The AHB bus will be reset when bit [0] is set to 1
3	HST_CORE_ RST_MSK	R/W	0x0	Used to specify the CPU core reset mask	
				0	CPU core module will not be reset when bit [0] is set to 1
				1	CPU core module will be reset when bit [0] is set to 1
2	HST_DMA_RST _MSK	R/W	0x0	Specifies the host DMA controller reset mask	
				0	The host DMA controller module will not be reset when bit [0] is set to 1
				1	The host DMA controller module will be reset when bit [0] is set to 1
1	WLAN_RST_ MSK	R/W	0x0	Specifies the WLAN reset mask.	
				0	WLAN module will not be reset when bit [0] is set to 1
				1	WLAN module will be reset when bit [0] is set to 1
0	WHOLE_CHIP_ RESET	R/W	0x0	A S/W programmable bit to reset those modules which set the mask values.	
				0	Reset deasserted
				1	Reset asserted

6.2.11 USB PLL Parameter Register

Address: 0x0005_0048
Access: Read/Write

This register is used to set the parameters for the USB PLL.

Bit	Bit Name	Type	Reset	Description	
31	INVPLLUSB OUT	R/W	0x0	Output inverse setting	
30	SVREG	R/W	0x1	Regulator output VDDvco level select	
				0	1.349 V
				1	1.246 V
29:27	SCLAMP	R/W	0x5	Control voltage Vc clamp current select. Default: 56.25 uA.	
26:24	ICP	R/W	0x6	Charge pump current select. Default: 34.375 uA.	
23:16	FILTER	R/W	0x15	Loop filter setting. Default: Rp = 12.5 KΩ; Cp = 112.5 pF; Cs = 12.5 pF	
15:14	ATB	R/W	0x0	Analog bus select. MSB:Vc; LSB:VDDvco	
13:4	DIV	R/W	0x1E	Feedback divider setting	
3:0	REFDIV	R/W	0x5	Reference divider setting	

6.2.12 Reset Status Register

Address: 0x0005_004C
Access: Read/Write

This register is used to denote the reset status.

Bit	Bit Name	Type	Reset	Description
31:0	RST_STATUS	R/W	0x0	Reset status

6.2.13 Chip Revision ID (RST_REVISION_ID)

Address: 0x0005_0090
Access: Read-Only

This register is used to denote the chip revision ID.

Bit	Bit Name	Type	Reset	Description
31:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:4	MAJOR	R	0xC	Major revision
3:0	MINOR	R	0x0	Minor revision

6.3 USB Controller DMA Registers

This section describes the Reset Clock Control registers for the AR9271. Table 6-4 defines the offset, type and page location of these registers.

Table 6-4. **USB Controller DMA Registers**

Address	Description	Page
0x0005_5000	Interrupt Status Register	page 48
0x0005_5004	Interrupt Mask Register	page 49
0x0005_5800	USB Rx 0 Descriptor Start Address	page 49
0x0005_5804	USB Rx 0 DMA Start Register	page 50
0x0005_5808	USB Rx 0 AHB Burst Size Register	page 50
0x0005_580C	USB Rx 0 Packet Offset Register	page 50
0x0005_581C	Rx Chain 0 Data Swap Register	page 50
0x0005_5900	USB Rx 1 Descriptor Start Address	page 50
0x0005_5904	USB Rx 1 DMA Start Register	page 51
0x0005_5908	USB Rx 1 AHB Burst Size Register	page 51
0x0005_590C	USB Rx 1 Packet Offset Register	page 51
0x0005_591C	Rx Chain 1 Data Swap Register	page 51
0x0005_5A00	USB Rx 2 Descriptor Start Address	page 52
0x0005_5A04	USB Rx 2 DMA Start Register	page 52
0x0005_5A08	USB Rx 2 AHB Burst Size Register	page 52
0x0005_5A0C	USB Rx 2 Packet Offset Register	page 52
0x0005_5A1C	Rx Chain 2 Data Swap Register	page 52
0x0005_5C00	USB Tx 0 Descriptor Start Address	page 53
0x0005_5C04	USB Tx 0 DMA Start Register	page 53
0x0005_5C08	USB Tx 0 Interrupt Limit Register	page 53
0x0005_5C0C	USB Tx 0 AHB Burst Size Register	page 53
0x0005_5C18	Tx Chain 0 AHB Burst Size Register	page 53

6.3.1 Interrupt Status Register (USB_DMA_INTERRUPT)

Address: 0x0005_5000
Access: Read-Only

This register is used to denote the interrupts produced on Tx/Rx chains.

Bit	Bit Name	Type	Reset	Description
31:25	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
24	TX_0_END	R	0x0	The DMA engine has reached the end of the descriptor chain on Tx chain 0
23:17	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	TX_0_ COMPLETE	R	0x0	A packet has been received on Tx chain 0
15:11	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
10	RX_2_END	R	0x0	The DMA engine has reached the end of the descriptor chain on Rx chain 2
9	RX_1_END	R	0x0	The DMA engine has reached the end of the descriptor chain on Rx chain 1

8	RX_0_END	R	0x0	The DMA engine has reached the end of the descriptor chain on Rx chain 0
7:3	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	RX_2_ COMPLETE	R	0x0	A packet has been received on Rx Chain 2
1	RX_1_ COMPLETE	R	0x0	A packet has been received on Rx Chain 1
0	RX_0_ COMPLETE	R	0x0	A packet has been received on Rx Chain 0

6.3.2 Interrupt Mask Register (USB_DMA_INTERRUPT_MASK)

Address: 0x0005_5004
Access: Read/Write

This register enables or disables propagation of interrupts in the Interrupt Register.

Bit	Bit Name	Type	Reset	Description
31:25	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
24	TX_0_END_MASK	R/W	0x0	Enables TX_0_END Interrupt if this bit is set as 1
23:17	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
16	TX_0_COMPLETE_ MASK	R/W	0x0	Enables TX_0_COMPLETE Interrupt if this bit is set as 1
15:11	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
10	RX_2_END_MASK	R/W	0x0	Enables RX_2_END Interrupt if this bit is set as 1
9	RX_1_END_MASK	R/W	0x0	Enables RX_1_END Interrupt if this bit is set as 1
8	RX_0_END_MASK	R/W	0x0	Enables RX_0_END Interrupt if this bit is set as 1
7:3	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	RX_2_ COMPLETE_MASK	R/W	0x0	Enables RX_2_COMPLETE Interrupt if this bit is set as 1
1	RX_1_ COMPLETE_MASK	R/W	0x0	Enables RX_1_COMPLETE Interrupt if this bit is set as 1
0	RX_0_ COMPLETE_MASK	R/W	0x0	Enables RX_0_COMPLETE Interrupt if this bit is set as 1

6.3.3 USB Rx Chain 0 Descriptor Start Address Register (USB_DMA_RX_0_DESC_START_ADDRESS)

Address: 0x0005_5800
Access: Read/Write

This register contains the address at the start of the descriptor chain. This register only needs to be set once after reset.

Bit	Bit Name	Type	Reset	Description
31:0	ADDRESS	R/W	0x0	The address at the start of the descriptor chain

6.3.4 USB Rx Chain 0 DMA Start Register (USB_DMA_RX_0_DMA_START)

Address: 0x0005_5804
Access: Read/Write

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	START	R/W	0x0	Writing a 1 to this bit will start the DMA chain if it is stopped. The bit will be cleared once the DMA engine has stopped and restarted.

6.3.5 USB Rx Chain 0 AHB Burst Size Register (USB_DMA_RX_0_BURST_SIZE)

Address: 0x0005_5808
Access: Read/Write

This register sets the standard DMA burst size used on the AHB bus.

00 = 4 words/16 bytes

01 = 8 words/32 bytes

10 = 16 words/64 bytes

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
1:0	BURST	R/W	0x0	Burst size

6.3.6 USB Rx Chain 0 Packet Offset Register (USB_DMA_RX_0_PKT_OFFSET)

Address: 0x0005_580C
Access: Read/Write

This register tells the DMA engine to place the packet at a programmable number of bytes after the start of the buffer. This allows the software to add an additional header in front of the packet without doing a copy.

Bit	Bit Name	Type	Reset	Description
31:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	OFFSET	R/W	0x0	The offset in bytes. The size of the buffer attached to the first descriptor of the packet must be larger than the offset value.

6.3.7 Rx Chain 0 Data Swap Register (USB_RX_0_DATA_SWAP)

Address: 0x0005_581C
Access: Read/Write

This register is used to swap information, if necessary, before sending it on.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	SWAP	R/W	0x0	This bit controls whether the data is swapped before sending it on.

6.3.8 USB Rx Chain 1 Descriptor Start Address Register (USB_DMA_RX_1_DESC_START_ADDRESS)

Address: 0x0005_5900
Access: Read/Write

This register contains the address at the start of the descriptor chain. This register only needs to be set once after reset.

Bit	Bit Name	Type	Reset	Description
31:0	ADDRESS	R/W	0x0	The address at the start of the descriptor chain

6.3.9 USB Rx Chain 1 DMA Start Register (USB_DMA_RX_1_DMA_START)

Address: 0x0005_5904
Access: Read/Write

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	START	R/W	0x0	Writing a 1 to this bit will start the DMA chain if it is stopped. The bit will be cleared once the DMA engine has stopped and restarted.

6.3.10 USB Rx Chain 1 AHB Burst Size Register (USB_DMA_RX_1_BURST_SIZE)

Address: 0x0005_5908
Access: Read/Write

This register sets the standard DMA burst size used on the AHB bus.

00 = 4 words/16 bytes

01 = 8 words/32 bytes

10 = 16 words/64 bytes

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
1:0	BURST	R/W	0x0	Burst size

6.3.11 USB Rx Chain 1 Packet Offset Register (USB_DMA_RX_1_PKT_OFFSET)

Address: 0x0005_590C
Access: Read/Write

This register tells the DMA engine to place the packet at a programmable number of bytes after the start of the buffer. This allows the software to add an additional header in front of the packet without doing a copy.

Bit	Bit Name	Type	Reset	Description
31:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	OFFSET	R/W	0x0	The offset in bytes. The size of the buffer attached to the first descriptor of the packet must be larger than the offset value.

6.3.12 Rx Chain 1 Data Swap Register (USB_RX_DATA_SWAP)

Address: 0x0005_591C
Access: Read/Write

This register is used to swap information, if necessary, before sending it on.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	SWAP	R/W	0x0	This bit controls whether the data is swapped before sending it on.

6.3.13 USB Rx Chain 2 Descriptor Start Address Register (USB_DMA_RX_2_DESC_START_ADDRESS)

Address: 0x0005_5A00
Access: Read/Write

This register contains the address at the start of the descriptor chain. This register only needs to be set once after reset.

Bit	Bit Name	Type	Reset	Description
31:0	ADDRESS	R/W	0x0	The address at the start of the descriptor chain

6.3.14 USB Rx Chain 2 DMA Start Register (USB_DMA_RX_2_DMA_START)

Address: 0x0005_5A04
Access: Read/Write

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	START	R/W	0x0	Writing a 1 to this bit will start the DMA chain if it is stopped. The bit will be cleared once the DMA engine has stopped and restarted.

6.3.15 USB Rx Chain 2 AHB Burst Size Register (USB_DMA_RX_2_BURST_SIZE)

Address: 0x0005_5A08
Access: Read/Write

This register sets the standard DMA burst size used on the AHB bus.

00 = 4 words/16 bytes

01 = 8 words/32 bytes

10 = 16 words/64 bytes

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
1:0	BURST	R/W	0x0	Burst size

6.3.16 USB Rx Chain 2 Packet Offset Register (USB_DMA_RX_2_PKT_OFFSET)

Address: 0x0005_5A0C
Access: Read/Write

This register tells the DMA engine to place the packet at a programmable number of bytes after the start of the buffer. This allows the software to add an additional header in front of the packet without doing a copy.

Bit	Bit Name	Type	Reset	Description
31:8	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
7:0	OFFSET	R/W	0x0	The offset in bytes. The size of the buffer attached to the first descriptor of the packet must be larger than the offset value.

6.3.17 Rx Chain 2 Data Swap Register (USB_RX_2_DATA_SWAP)

Address: 0x0005_5A1C
Access: Read/Write

This register is used to swap information, if necessary, before sending it on.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	SWAP	R/W	0x0	This bit controls whether the data is swapped before sending it on.

6.3.18 USB Tx Chain 0 Descriptor Start Address Register (USB_DMA_TX_0_DESC_START_ADDRESS)

Address: 0x0005_5C00
Access: Read/Write

This register contains the address at the start of the descriptor chain. This register only needs to be set once after reset.

Bit	Bit Name	Type	Reset	Description
31:0	ADDRESS	R/W	0x0	The address at the start of the descriptor chain

6.3.19 USB Tx Chain 0 DMA Start Register (USB_DMA_TX_0_DMA_START)

Address: 0x0005_5C04
Access: Read/Write

This register is used to start or resume reading the descriptor chain.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	START	R/W	0x0	Writing a 1 to this bit will start the DMA chain if it is stopped. The bit will be cleared once the DMA engine has stopped and restarted.

6.3.20 USB Tx Chain 0 Interrupt Limit Register (USB_DMA_TX_0_INTERRUPT_LIMIT)

Address: 0x0005_5C08
Access: Read/Write

This register contains limits that set how often the COMPLETE interrupt is asserted.

Bit	Bit Name	Type	Reset	Description
31:16	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
15:4	TIMEOUT	R/W	0x0	This value sets the maximum time the DMA engine will wait before asserting an interrupt after a packet has been received. This time limit is set in units of 32 clock cycles.
3:0	COUNT	R/W	0x1	In the absence of a timeout, an interrupt will be asserted after this many packets since the last time the interrupt register was read.

6.3.21 Tx Chain 0 AHB Burst Size Register (USB_DMA_TX_0_BURST_SIZE)

Address: 0x0005_5C0C
Access: Read/Write

This register sets the standard DMA burst size used on the AHB bus.

00 = 4 words/16 bytes

01 = 8 words/32 bytes

10 = 16 words/64 bytes

Bit	Bit Name	Type	Reset	Description
31:2	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
1:0	BURST	R/W	0x0	Burst size

6.3.22 Tx Chain 0 Data Swap Register (USB_TX_0_DATA_SWAP)

Address: 0x0005_5C18
Access: Read/Write

This register is used to swap information, if necessary, before sending it on.

Bit	Bit Name	Type	Reset	Description
31:1	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
0	SWAP	R/W	0x0	This bit controls whether the data is swapped before sending it on.

6.4 SPI Control Registers

This section describes the SPI registers for the AR9271. Table 6-5 defines the offset, type and page location of these registers.

Table 6-5. **SPI Control Registers**

Offset	Description	Page
0x0005_B000	SPI Control/Status Register	page 55
0x0005_B004	SPI Address/Opcode Register	page 55
0x0005_B008	SPI Data Register	page 56

SPI Control Register Notes

An SPI transaction consists of three phases: an opcode transmit phase (always a single byte), followed by an optional address transmit phase of 0-3 bytes, followed by an optional data transmit or receive phase of 0-4 bytes. Then, an SPI transaction consists of a 1- to 8-byte transmit phase to the SPI device, followed by a 0- to 8-byte receive phase from the SPI device.

The ‘transmit byte count’ field in the SPI_CS register controls the size (number of bytes) of the transmit phase. The source of each of the bytes transmitted is fixed, as the following table denotes.

Table 6-6. **SPI Source Bytes Table**

Byte	Source
0	SPI_AO [7:0] (the ‘SPI opcode’ field)
1	SPI_AO [31:24] (the high byte of the ‘SPI address’ field)
2	SPI_AO [23:16] (the middle byte of the ‘SPI address’ field)
3	SPI_AO [15:8] (the low byte of the ‘SPI address’ field)
4	SPI_D [7:0] (the low byte of the ‘SPI data’ register)
5	SPI_D [15:8] (the next byte of the ‘SPI data’ register)
6	SPI_D [23:16] (the next byte of the ‘SPI data’ register)
7	SPI_D [31:24] (the high byte of the ‘SPI data’ register)

The ‘receive byte count’ field in the SPI_CS register controls the size (number of bytes) of the receive phase. The destination of each of the bytes received is fixed, as the following table denotes.

Table 6-7. **SPI Destination Bytes Table**

Byte	Source
0	SPI_D [7:0] (the low byte of the ‘SPI data’ register)
1	SPI_D [15:8] (the next byte of the ‘SPI data’ register)
2	SPI_D [23:16] (the next byte of the ‘SPI data’ register)
3	SPI_D [31:24] (the high byte of the ‘SPI data’ register)
4	SPI_AO [7:0] (the ‘SPI opcode’ field)
5	SPI_AO [15:8] (the low byte of the ‘SPI address’ field)
6	SPI_AO [23:16] (the middle byte of the ‘SPI address’ field)
7	SPI_AO [31:24] (the high byte of the ‘SPI address’ field)

To perform an SPI transaction:

1. Write the appropriate values into the SPI_AO and SPI_D registers.

2. Write the appropriate values into the ‘transmit byte count’ and ‘received byte count’ fields of the SPI_CS register.

3. Write a ‘1’ into the ‘SPI transaction start’ bit of the SPI_CS register (this step can be combined with the one above, if desired, so that only a single SPI_CS write is needed).

4. Poll the transaction busy indication’ bit in the SPI_CS register until it is clear.

5. If the transaction included a receive phase, then retrieve the received data by reading the appropriate bytes from the SPI_D and SPI_AO registers.

6.4.1 SPI Control/Status Register *(SPI_CS)*

Address: 0x0005_B000
Access: Read/Write

This register is used to set the SPI transaction parameters.

Bit	Bit Name	Type	Reset	Description
31:19	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
18:17	SPI_AUTO_ SIZE	R	0x1	Indicates the SPI address size is 24 bits
16	SPI_BUSY	R	0x0	Transaction busy indication 0: No SPI transaction is ongoing. Software may start a new SPI transaction by writing to the ‘SPI transaction start’ bit within this register. 1: An SPI transaction is currently ongoing. Software must not try to start a new SPI transaction, nor may the software alter the value of any field of the SPI_CS, SPI_AO or the SPI_D registers.
15:9	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
8	SPI_START	R/W	0x0	SPI transaction start. Only writes to this field are valid. Reads will always return a zero. For writes: A write of 1 starts the SPI transaction defined by the transmit byte count, receive byte count, SPI_AO, and SPI_D registers. A write of 0 has no effect
7:4	RX_CNT	R/W	0xX	Receive byte count. Determines the number of bytes received from the SPI device. Values between 1-8 are valid, and other values are illegal.
3:0	TX_CNT	R/W	0xX	Transmit byte count. Determines the number of bytes transmitted to the SPI device. Values between 1-8 are valid, and other values are illegal.

6.4.2 SPI Address/Opcode Register (SPI_AO)

Address: 0x0005B004
Access: Read/Write

This register is used to specify the SPI address for transaction.

Bit	Bit Name	Type	Reset	Description
31:8	SPI_ADDR	R/W	0xX	SPI Address. This field usually specifies the 24-bit address to transmit to the SPI device. See the previous “SPI Control Register Notes” on page 54 for more information.
7:0	SPI_OPCODE	R/W	0xX	SPI Opcode. This field usually specifies the 8-bit instruction to transmit to the SPI device as the first part of an SPI transaction.

6.4.3 SPI Data Register (SPI_D)

Address: 0x0005B008
Access: Read/Write

This register is sued to transmit data bytes to or from the SPI device.

Bit	Bit Name	Type	Reset	Description
31:0	SPI_DATA	R/W	0xX	SPI data. This register usually specifies a series of up to four data bytes to transmit to or receive from the SPI device.

MAC Register Descriptions

This section describes the AR9271 MAC registers.

Address	Type	Page
0x1000_0000 – 0x1000_00FC	General DMA and Rx-Related (MAC Interface)	page 57
0x1000_0800 – 0x1000_0FFC	QCU	page 76
0x1000_1000 – 0x1000_12FC	DCU	page 83
0x1000_4000 – 0x1000_40FC	Host Interface Registers	page 93
0x1000_7000 – 0x1000_7FFC	RTC Interface	page 104
0x1000_8000 – 0x1000_97FC	MAC PCU	page 108

6.5 General DMA and Rx-Related Registers

Table 6-8 shows the mapping of the general DMA and Rx-related (MAC interface) registers.

Table 6-8. **General DMA and Rx-Related Registers**

Address	Name	Description	Page
0x1000_0008	CR	Command	page 58
0x1000_000C	RXDP	Receive Queue Descriptor Pointer	page 58
0x1000_0014	CFG	Configuration and Status	page 59
0x1000_0020	MIRT	Maximum Interrupt Rate Threshold	page 60
0x1000_0024	IER	Interrupt Global Enable	page 60
0x1000_0028	TIMT	Transmit Interrupt Mitigation Thresholds	page 60
0x1000_002C	RIMT	Receive Interrupt Mitigation Thresholds	page 61
0x1000_0030	TXCFG	Transmit Configuration	page 61
0x1000_0034	RXCFG	Receive Configuration	page 62
0x1000_0040	MIBC	MIB Control	page 62
0x1000_0044	TOPS	Timeout Prescale	page 62
0x1000_0048	RXNF	Rx No Frame	page 63
0x1000_004C	TXNF	Tx No Frame	page 63
0x1000_0050	RFGTO	Receive Frame Gap Timeout	page 63
0x1000_0054	RFCNT	Receive Frame Count Limit	page 63
0x1000_0064	GTT	Global Transmit Timeout	page 64
0x1000_0068	GTTM	Global Transmit Timeout Mode	page 64
0x1000_006C	CST	Carrier Sense Timeout	page 64
0x1000_0080	ISR_P	Primary Interrupt Status	page 65
0x1000_0084	ISR_S0	Secondary Interrupt Status 0	page 67
0x1000_0088	ISR_S1	Secondary Interrupt Status 1	page 67
0x1000_008C	ISR_S2	Secondary Interrupt Status 2	page 68
0x1000_0090	ISR_S3	Secondary Interrupt Status 3	page 68
0x1000_0094	ISR_S4	Secondary Interrupt Status 4	page 69
0x1000_0098	ISR_S5	Secondary Interrupt Status 5	page 69
0x1000_00A0	IMR_P	Primary Interrupt Mask	page 70
0x1000_00A4	IMR_S0	Secondary Interrupt Mask 0	page 71
0x1000_00A8	IMR_S1	Secondary Interrupt Mask 1	page 71

Table 6-8. **General DMA and Rx-Related Registers (continued)**

Address	Name	Description	Page
0x1000_00AC	IMR_S2	Secondary Interrupt Mask 2	page 72
0x1000_00B0	IMR_S3	Secondary Interrupt Mask 3	page 72
0x1000_00B4	IMR_S4	Secondary Interrupt Mask 4	page 73
0x1000_00B8	IMR_S5	Secondary Interrupt Mask 5	page 73
0x1000_00C0	ISR_P_RAC	Primary Interrupt Status Read-and-Clear	page 74
0x1000_00C4	ISR_S0_S	Secondary Interrupt Status 0 (Shadow Copy)	page 74
0x1000_00C8	ISR_S1_S	Secondary Interrupt Status 1 (Shadow Copy)	page 74
0x1000_00CC	ISR_S2_S	Secondary Interrupt Status 2 (Shadow Copy)	page 74
0x1000_00D0	ISR_S3_S	Secondary Interrupt Status 3 (Shadow Copy)	page 74
0x1000_00D4	ISR_S4_S	Secondary Interrupt Status 4 (Shadow Copy)	page 75
0x1000_00D8	ISR_S5_S	Secondary Interrupt Status 5 (Shadow Copy)	page 75

6.5.1 Command (CR)

Address: 0x1000_0008
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:7	RES	Reserved
6	SWI	Software interrupt; this bit is one-shot/auto-cleared, so it always reads as 0
5	RXD	Rx disable
4:3	RES	Reserved
2	RXE	Receive (Rx) enable
1:0	RES	Reserved

6.5.2 Rx Queue Descriptor Pointer (RXDP)

Address: 0x1000_000C
Access: Read/Write
Cold Reset: (Undefined)
Warm Reset: (Unaffected)

Bit	Name	Description
31:2	RXDP	Rx descriptor pointer
1:0	RES	Reserved

6.5.3 Configuration and Status (CFG)

Address: 0x1000_0014
Access: Read/Write
Cold Reset: See field description
Warm Reset: (Same as Cold Reset)

Bit	Name	Reset	Description	
31:19	RES	0x0	Reserved	
18:17	FULL_THRESHOLD	0x0	Request queue full threshold	
			0	Use default value of 4
			3:1	Use indicated value
16:13	RES	0x0	Reserved	
12	CFG_HALT_ACK	0x0	DMA halt status	
			0	DMA has not yet halted
			1	DMA has halted
11	CFG_HALT_REQ	0x0	DMA halt in preparation for reset request	
			0	DMA logic operates normally
			1	Request DMA logic to stop so software can reset the MAC Bit [12] of this register indicates when the halt has taken effect; the DMA halt IS NOT recoverable; once software sets bit [11] to request a DMA halt, software must wait for bit [12] to be set and reset the MAC.
10	CFG_CLKGATE_DIS	0x0	Clock gating disable	
			0	Allow clock gating in all DMA blocks to operate normally
			1	Disable clock gating in all DMA blocks (for debug use)
9	RES	0x0	Reserved	
8	RES	0x1	Reserved	
7:6	RES	0x0	Reserved	
5	REG_CFG_ADHOC	0x0	AP/ad hoc indication	
			0	AP mode MAC is operating either as an access point (AP) or as a station (STA) in a BSS
			1	Ad hoc mode MAC is operating as a STA in an independent basic service set (IBSS)
4	MODE_MMR	0x0	Byteswap register access (MMR) data words	
3	MODE_RCV_DATA	0x0	Byteswap Rx data buffer words	
2	MODE_RCV_DESC	0x0	Byteswap Rx descriptor words	
1	MODE_XMIT_DATA	0x0	Byteswap Tx data buffer words	
0	MODE_XMIT_DESC	0x0	Byteswap Tx descriptor words	

6.5.4 Maximum Interrupt Rate Threshold (MIRT)

Address: 0x1000_0020
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	RES	Reserved
15:0	INTR_RATE_THRESH	Maximum interrupt rate threshold This register is described in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The maximum interrupt rate timer is started when either the TXINTM or RXIMTM status bits are set. TXMINTR or RXMINTR are asserted at this time. No future TXINTM or RXINTM events can cause the TXMINTR or TXMINTR to be asserted until this timer has expired. If both the TXINTM and RXINTM status bits are set while the timer is expired then the TXMINTR and RXMINTR will round robin between the two.

6.5.5 Interrupt Global Enable (IER)

Address: 0x1000_0024
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:1	RES	Reserved
0	REG_IER	Enable hardware signalling of interrupts

6.5.6 Tx Interrupt Mitigation Thresholds (TIMT)

Address: 0x1000_0028
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	TX_FIRST_PKT_THRESH	Tx first packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx first packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The first Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.
15:0	TX_LAST_PKT_THRESH	Tx last packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The Tx last packet timer starts counting after any Tx completion. If the timer is still counting when the next Tx completion occurs, it resets and starts over. The last Tx packet timer expires when either the last Tx packet threshold equals the last Tx packet timer count or the first Tx packet threshold equals the first Tx packet timer count.

6.5.7 Rx Interrupt Mitigation Thresholds (RIMT)

Address: 0x1000_002C
Access: Read/Write
Cold Reset: (See Field Descriptions)
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	RX_FIRST_PKT_THRESH	Receive first packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The receive first packet timer starts counting after any receive completion. If the timer is still counting when the next receive completion occurs, it resets and starts over. The first receive packet timer expires when either the last receive packet threshold equals the last receive packet timer count or the first receive packet threshold equals the first receive packet timer count.
15:0	RX_LAST_PKT_THRESH	Receive last packet threshold This register is in µs up to a maximum of 65.535 ms. If this register is 0x0, the interrupt mitigation mechanism is disabled. The receive last packet timer starts counting after any receive completion. If the timer is still counting when the next receive completion occurs, it resets and starts over. The last receive packet timer expires when either the last receive packet threshold equals the last receive packet timer count or the first receive packet threshold equals the first receive packet timer count.

6.5.8 Tx Configuration (TXCFG)

Address: 0x1000_0030
Access: Read/Write
Cold Reset: (See Field Descriptions)
Warm Reset: (Same as Cold Reset)

Bit	Name	Reset	Description	
31:18	RES	0x0	Reserved	
17	DIS_RETRY_UNDERRUN	0x1	Disable retry of underrun packets	
			0	Underrun packets will retry indefinitely
			1	Underrun packets will quit after first underrun attempt and write status indicating underrun
16:10	RES	0x0	Reserved	
9:4	TXCFG_TRIGLVL	0x1	Frame trigger level Specifies the minimum number of bytes, in units of 64 bytes, that must be DMAed into the PCU TXFIFO before the PCU initiates sending the frame on the air. Resets to 0x1 (meaning 64B or a full frame, whichever occurs first).	
3	RES	0x0	Reserved	
2:0	TXCFG_DMA_SIZE	0x5	Maximum DMA request size for master reads	
			0	4 B
			1	8 B
			2	16 B
			3	32 B
			4	64 B
			5	128 B
			6	256 B
			7	Reserved

6.5.9 Rx Configuration (RXCFG)

Address: 0x1000_0034
Access: Read/Write
Cold Reset: (See Field Descriptions)
Warm Reset: (Same as Cold Reset)

Bit	Name	Reset	Description
31:5	RES	0x0	Reserved
4:3	ZERO_LEN_DMA_EN	0x0	Zero-length frame DMA enable 0 — Disable DMA of all zero-length frames. In this mode, the DMA logic suppresses all zero-length frames. Reception of zero-length frames is invisible to the host (they neither appear in host memory nor consume a Rx descriptor). 1 — Reserved 2 — Enable DMA of all zero-length frames. In this mode, all zero-length frames (chirps, double-chirps, and non-chirps) are DMAed into host memory just like normal (non-zero-length) frames. 3 — Reserved
2:0	DMA_SIZE	0x4	Maximum DMA size for master writes (See the encodings for the register "Tx Configuration (TXCFG)" on page 61)

6.5.10 MIB Control (MIBC)

Address: 0x1000_0040
Access: Read/Write
Cold Reset: (See Field Descriptions)
Warm Reset: (Same as Cold Reset)

Bit	Name	Reset	Description
31:4	RES	0x0	Reserved
3	MIBC_MIBS	0x0	MIB counter strobe. This bit is a one-shot and always reads as zero. For writes: 0 — No effect 1 — Causes every MIB counter to increment by one
2	MIBC_ACLR	0x1	Clear all counters
1	MIBC_FRZ	0x1	Freeze all counters
0	MIBC_WRN_COMP	0x0	Warning test indicator. Read Only

6.5.11 Timeout Prescale (TOPS)

Address: 0x1000_0044
Access: Read/Write
Cold Reset: 0x0000
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	RES	Reserved
15:0	TOPS	Timeout prescale count. Controls the prescale for interrupt-related timeouts. Set to 0 to disable.

6.5.12 Rx No Frame (RXNF)

Address: 0x1000_0048
Access: Read/Write
Cold Reset: 0x000
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:10	RES	Reserved
9:0	RXNPTO	Timeout count limit

6.5.13 Tx No Frame (TXNF)

Address: 0x1000_004C
Access: Read/Write
Cold Reset: 0x000
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:20	RES	Reserved
19:10	TXNPMASK	QCU mask Specifies the set of QCUs for which frame completions cause a reset of the TXNOFR timeout.
9:0	TXNPTO	Timeout count limit

6.5.14 Rx Frame Gap Timeout (RFGTO)

Address: 0x1000_0050
Access: Read/Write
Cold Reset: 0x000
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:10	RES	Reserved
9:0	RPGTO	Timeout count limit

6.5.15 Rx Frame Count Limit (RFCNT)

Address: 0x1000_0054
Access: Read/Write
Cold Reset: (See Field Descriptions)
Warm Reset: (Same as Cold Reset)

NOTE: Set to 0x1F (decimal 31) to disable.

Bit	Name	Reset	Description
31:5	RES	0x0	Reserved
4:0	RPCNT	0x1F	Frame count limit

6.5.16 Global Tx Timeout (GTT)

Address: 0x1000_0064
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	GTT_LIMIT	Timeout limit (in TU: 1024 µs) On reset, this value is set to 25 TU.
15:0	GTT_CNT	Timeout counter (in TU: 1024 µs) The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or else the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit, the global transmit timeout interrupt is set in the ISR. This mechanism can be used to detect whether a Tx frame is ready and is unable to be transmitted.

6.5.17 Global Tx Timeout Mode (GTTM)

Address: 0x1000_0068
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:5	RES	Reserved
4	GTT_QCU_FR_DISABLE	Disable QCU_FR_ACTIVE for GTT If this bit is set, then GTT logic uses the TX_QCU_STATUS signal for GTT. If this bit is clear, then QCU_FR_ACTIVE is used instead.
3	CST_USEC_STROBE	CST µs strobe If this bit is set, then the CST timer will not use the TU based strobe but rather use the µs strobe to increment the timeout counter.
2	RESET_ON_CHAN_IDLE	Reset count on chan idle low. Reset count every time channel idle is low.
1	IGNORE_CHAN_IDLE	Ignore channel idle If this bit is set then the GTT timer does not increment if the channel idle indicates the air is busy or NAV is still counting down.
0	USEC_STROBE	µs strobe If this bit is set then the GTT timer will not use the TU based strobe but rather use a µs strobe to increment the timeout counter.

6.5.18 Carrier Sense Timeout (CST)

Address: 0x1000_006C
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:16	CST_LIMIT	Timeout limit (in TU: 1024 µs). On reset, this value is set to 16 TU.
15:0	CST_CNT	Timeout counter (in TU: 1024 µs) The current value of the timeout counter that is reset on every transmit. If no Tx frame is queued up and ready to transmit, the timeout counter stays at 0 or the counter increments every 1024 µs. If the timeout counter is equal to or greater than the timeout limit then carrier sense timeout (CST) interrupt is set in the ISR. This counter starts counting if any queues are ready for Tx. It continues counting when RX_CLEAR is low, which is useful to determine whether the transmit is stuck because RX_CLEAR is low for a long time.

6.5.19 Primary Interrupt Status (ISR_P)

Address: 0x1000_0080
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

NOTE:

- The bits that are logical ORs of bits in the secondary ISRs are generated by logically ORing the secondary ISR bits after the secondary ISR bits have been masked with the appropriate bits from the corresponding secondary interrupt mask register.
- A write of one to a bit that is a logical OR of bits in a secondary ISR clears the secondary ISR bits from which the primary ISR bit is generated. E.g.: A write of a one to the TXOK bit (bit [6]) in ISR_P clears all 10 TXOK bits in ISR_S0 (bits [9:0] of "Secondary Interrupt Status 0 (ISR_S0)").
- Only the bits in this register (ISR_P) and the primary interrupt mask register ("Primary Interrupt Mask (IMR_P)") control whether the MAC's interrupt output is asserted. The bits in the several secondary interrupt status/mask registers control what bits are set in the primary interrupt status register; however, the IMR_S* registers do not determine whether an interrupt is asserted. That is, an interrupt is asserted only when the logical AND of ISR_P and IMR_P is non-zero. The secondary interrupt mask/status registers affect which bits are set in ISR_P, but do not directly affect whether an interrupt is asserted.

Bit	Name	Description
31	RXINTM	Rx completion interrupt after mitigation; either the first Rx packet or last Rx packet interrupt mitigation count has reached its threshold (see the register "Rx Interrupt Mitigation Thresholds (RIMT)" on page 61)
30	TXINTM	Tx completion interrupt after mitigation; either the first Tx packet or last Tx packet interrupt mitigation count has reached its threshold (see the register "Tx Interrupt Mitigation Thresholds (TIMT)" on page 60)
29	HCFTO	HCF poll timeout
28	GENTMR	Logical OR of all GENERIC TIMER bits in the secondary ISR 5 which include the GENERIC_TIMER_TRIGGER[7:0], GENERIC_TIMER_THRESH[7:0], GENERIC_TIMER_OVERFLOW
27	QTRIG	Logical OR of all QTRIG bits in secondary ISR 4; indicates that at least one QCU's frame scheduling trigger event has occurred
26	QCBRURN	Logical OR of all QCBRURN bits in secondary ISR 3; indicates that at least one QCU's frame scheduling trigger event occurred when no frames were present on the queue
25	QCBROVF	Logical OR of all QCBROVF bits in secondary ISR 3; indicates that at least one QCU's CBR expired counter has reached the value of the QCU's cbr_ovf_thresh parameter
24	RXMINTR	RXMINTR maximum receive interrupt rate; same as RXINTM with the added requirement that maximum interrupt rate count has reached its threshold; this interrupt alternates with TXMINTR.
23	BCNMISC	Miscellaneous beacon-related interrupts This bit is the logical OR of the CST, GTT, TIM, CABEND, DTIMSYNC, BCNTO, CABTO, TSFOOR, DTIM, and TBTT_TIME bits in secondary ISR 2.
22	HCFPOLL	Received directed HCF poll
21	RES	Reserved
20	BNR	Beacon not ready Indicates that the QCU marked as being used for beacons received a DMA beacon alert when the queue contained no frames.

Bit	Name	Description
19	TXMINTR	TXMINTR maximum Tx interrupt rate
18	BMISS	The PCU indicates that it has not received a beacon during the previous *N* (*N* is programmable) beacon periods
17	BRSSI	The PCU indicates that the RSSI of a beacon it has received has fallen below a programmable threshold
16	SWBA	The PCU has signalled a software beacon alert
15	RXKCM	Key cache miss; a frame was received with a set key cache miss Rx status bit
14	RXPHY	The PHY signalled an error on a received frame
13	SWI	Software interrupt signalled; see the register "Command (CR)" on page 58
12	MIB	One of the MIB registers has reached its threshold
11	TXURN	Logical OR of all TXURN bits in secondary ISR 2. Indicates that the PCU reported a txfifo underrun for at least one QCU's frame
10	TXEOL	Logical OR of all TXEOL bits in secondary ISR 1; indicates that at least one Tx descriptor fetch state machine has no more Tx descriptors available
9	TXNOFR	Have not transmitted a frame in TXNOFR timeout clocks. Each QCU has only one TXNOFR bit; see the register "Tx No Frame (TXNF)" on page 63
8	TXERR	Logical OR of all TXERR bits in secondary ISR 1; indicates that at least one frame was completed with an error, regardless of whether the InterReq bit was set
7	TXDESC	Logical OR of all TXDESC bits in secondary ISR 0; indicates that at least one frame was sent and last descriptor had the InterReq bit set
6	TXOK	Logical OR of all TXOK bits in secondary ISR 0; indicates that at least one frame was completed with no errors and at the requested rate, regardless of whether the InterReq bit was set.
5	RXORN	Rxfifo overrrun
4	RXEOL	Rx descriptor fetch logic has no more Rx descriptors available
3	RXNOFR	No frame was received for RXNOFR timeout clocks
2	RXERR	The frame was received with errors
1	RXDESC	The frame was received and the InterReq field in the Rx descriptor was such that an interrupt was generated
0	RXOK	The frame was received with no errors

6.5.20 Secondary Interrupt Status 0 (ISR_S0)

Address: 0x1000_0084
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	TXDESC for QCU 9
...	...
17	TXDESC for QCU 1
16	TXDESC for QCU 0
15:10	Reserved
9	TXOK for QCU 9
...	...
1	TXOK for QCU 1
0	TXOK for QCU 0

6.5.21 Secondary Interrupt Status 1 (ISR_S1)

Address: 0x1000_0088
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	TXEOL for QCU 9
...	...
17	TXEOL for QCU 1
16	TXEOL for QCU 0
15:10	Reserved
9	TXERR for QCU 9
...	...
1	TXERR for QCU 1
0	TXERR for QCU 0

6.5.22 Secondary Interrupt Status 2 (ISR_S2)

Address: 0x1000_008C
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31	TBTT_TIME	TBTT-referenced timer interrupt; indicates the PCU’s TBTT-referenced timer has elapsed.
30	TSFOOR	TSF out of range; indicates that the corrected TSF received from a beacon differs from the PCU's internal TSF by more than a (programmable) threshold
29	DTIM	A beacon was received with the DTIM bit set and a DTIM count value of zero. Beacons with a set DTIM bit but a non-zero DTIM count do not generate it.
28	CABTO	CAB timeout; a beacon was received that indicated that the STA should expect to receive CAB traffic. However, the PCU's CAB timeout expired either because the station received no CAB traffic, or because the STA received some CAB traffic but never received a CAB frame with the more data bit clear in the frame control field (which would indicate the final CAB frame).
27	BCNTO	Beacon timeout; a TBTT occurred and the STA began waiting to receive a beacon, but no beacon was received before the PCU’s beacon timeout expired
26	DTIMSYNC	DTIM synchronization lost; a beacon was received that was expected to be a DTIM but was not, or a beacon was received that was not expected to be a DTIM but was
25	CABEND	End of CAB traffic; a CAB frame was received with the more data bit clear in the frame control field
24	TIM	A beacon was received with the local station's bit set in the TIM element
23	GTT	Global Tx timeout; indicates the GTT count ≥ the GTT limit
22	CST	Carrier sense timeout; indicates the CST count ≥ the CST limit
21:10	Reserved	
9	TXURN for QCU 9	
...	...	
1	TXURN for QCU 1	
0	TXURN for QCU 0	

6.5.23 Secondary Interrupt Status 3 (ISR_S3)

Address: 0x1000_0090
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	QCBRURN for QCU 9
...	...
17	QCBRURN for QCU 1
16	QCBRURN for QCU 0
15:10	Reserved
9	QCBROVF for QCU 9
1	QCBROVF for QCU 1
...	...
0	QCBROVF for QCU 0

6.5.24 Secondary Interrupt Status 4 (ISR_S4)

Address: 0x1000_0094
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:10	Reserved
9	QTRIG for QCU 9
...	...
1	QTRIG for QCU 1
0	QTRIG for QCU 0

6.5.25 Secondary Interrupt Status 5 (ISR_S5)

Address: 0x1000_0094
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

NOTE: The trigger indicates that the TSF matched or exceeded the timer. The threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The GENERIC_TIMER 0 threshold was removed because timer 0 is special and does not generate threshold event.

Bit	Description
31	GENERIC_TIMER 15 threshold
...	...
17	GENERIC_TIMER 1 threshold
16	GENERIC_TIMER overflow
15	GENERIC_TIMER 15 trigger
...	...
1	GENERIC_TIMER 1 trigger
0	GENERIC_TIMER 0 trigger

6.5.26 Primary Interrupt Mask (IMR_P)

Address: 0x1000_00A0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

NOTE: Only the bits in this register control whether the MAC's interrupt outputs are asserted. The bits in the secondary interrupt mask registers control what bits are set in the "Primary Interrupt Status (ISR_P)" on page 65 register; however, the IMR_S* registers do not determine whether an interrupt is asserted.

Bit	Description
31	RXINTM interrupt enable
30	TXINTM interrupt enable
29	HCFTO interrupt enable
28	GENTMR interrupt enable
27	QTRIG interrupt enable
26	QCBRURN interrupt enable
25	QCBROVF interrupt enable
24	RXMINTR interrupt enable
23	BCNMISC interrupt enable
22	HCFPOLL interrupt enable
21	Reserved
20	BNR interrupt enable
19	TXMINTR interrupt enable
18	BMISS interrupt enable
17	BRSSI interrupt enable
16	SWBA interrupt enable
15	RXKCM interrupt enable
14	RXPHY interrupt enable
13	SWI interrupt enable
12	MIB interrupt enable
11	TXURN interrupt enable
10	TXEOL interrupt enable
9	TXNOFR interrupt enable
8	TXERR interrupt enable
7	TXDESC interrupt enable
6	TXOK interrupt enable
5	RXORN interrupt enable
4	RXEOL interrupt enable
3	RXNOFR interrupt enable
2	RXERR interrupt enable
1	RXDESC interrupt enable
0	RXOK interrupt enable

6.5.27 Secondary Interrupt Mask 0 (IMR_S0)

Address: 0x1000_00A4
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	TXDESC for QCU 9 interrupt enable
...	...
17	TXDESC for QCU 1 interrupt enable
16	TXDESC for QCU 0 interrupt enable
15:10	Reserved
9	TXOK for QCU 9 interrupt enable
...	...
1	TXOK for QCU 1 interrupt enable
0	TXOK for QCU 0 interrupt enable

6.5.28 Secondary Interrupt Mask 1 (IMR_S1)

Address: 0x1000_00A8
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	TXEOL for QCU 9 interrupt enable
...	...
17	TXEOL for QCU 1 interrupt enable
16	TXEOL for QCU 0 interrupt enable
15:10	Reserved
9	TXERR for QCU 9 interrupt enable
...	...
1	TXERR for QCU 1 interrupt enable
0	TXERR for QCU 0 interrupt enable

6.5.29 Secondary Interrupt Mask 2 (IMR_S2)

Address: 0x1000_00AC
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31	TBTT_TIME interrupt enable	
30	TSFOOR interrupt enable	
29	DTIM interrupt enable	
28	CABTO interrupt enable	
27	BCNTO interrupt enable	
26	DTIMSYNC interrupt enable	
25	CABEND interrupt enable	
24	TIM interrupt enable	
23	GTT interrupt enable	
22	CST interrupt enable	
21:10	Reserved	
9	TXURN for QCU 9 interrupt enable	
...	...	
1	TXURN for QCU 1 interrupt enable	
0	TXURN for QCU 0 interrupt enable	

6.5.30 Secondary Interrupt Mask 3 (IMR_S3)

Address: 0x1000_00B0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:26	Reserved
25	QCBRURN for QCU 9 interrupt enable
...	...
17	QCBRURN for QCU 1 interrupt enable
16	QCBRURN for QCU 0 interrupt enable
15:10	Reserved
9	QCBROVF for QCU 9 interrupt enable
...	...
1	QCBROVF for QCU 1 interrupt enable
0	QCBROVF for QCU 0 interrupt enable

6.5.31 Secondary Interrupt Mask 4 (IMR_S4)

Address: 0x1000_00B4
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Description
31:10	Reserved
9	QTRIG for QCU 9 interrupt enable
...	...
1	QTRIG for QCU 1 interrupt enable
0	QTRIG for QCU 0 interrupt enable

6.5.32 Secondary Interrupt Mask 5 (IMR_S5)

Address: 0x1000_00B8
Access: Read/Write-One-to-Clear
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

NOTE: The trigger indicates the TSF matched or exceeded the timer; threshold is set when the TSF exceeds the timer by the GENERIC_TIMER_THRESH value. The GENERIC_TIMER overflow occurs when the TSF exceeds the timer by such a large amount that TSF ≥ Timer + Period, indicating incorrect software programming. The threshold GENERIC_TIMER 0 was removed because timer 0 is special and does not generate a threshold event.

Bit	Description
31	GENERIC_TIMER_THRESHOLD 15
30	GENERIC_TIMER_THRESHOLD 14
...	
18	GENERIC_TIMER_THRESHOLD 2
17	GENERIC_TIMER_THRESHOLD 1
16	GENERIC_TIMER overflow enable
15	GENERIC_TIMER 15 trigger enable
...	...
1	GENERIC_TIMER 1 trigger enable
0	GENERIC_TIMER 0 trigger enable

6.5.33 *Primary Interrupt Status Read and Clear (ISR_P_RAC)*

Address: 0x1000_00C0
Access: Read-and-Clear (No Write Access)
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

NOTE: A read from this location atomically:

- Copies all secondary ISRs into the corresponding secondary ISR shadow registers (ISR_S0 is copied to ISR_S0_S, etc.)
- Clears all bits of the primary ISR (ISR_P) and all bits of all secondary ISRs (ISR_S0–ISR_S4)
- Returns the contents of the primary ISR (ISR_P)

Bit	Name	Description
31:0	ISR_P	Same format as "Primary Interrupt Status (ISR_P)"

6.5.34 *Secondary Interrupt Status 0 (ISR_S0_S)*

Address: 0x1000_00C4
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S0	Same format as "Secondary Interrupt Status 0 (ISR_S0)"

6.5.35 *Secondary Interrupt Status 1 (ISR_S1_S)*

Address: 0x1000_00C8
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S1	Same format as "Secondary Interrupt Status 1 (ISR_S1)"

6.5.36 *Secondary Interrupt Status 2 (ISR_S2_S)*

Address: 0x1000_00CC
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S2	Same format as "Secondary Interrupt Status 2 (ISR_S2)"

6.5.37 *Secondary Interrupt Status 3 (ISR_S3_S)*

Address: 0x1000_00D0
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S3	Same format as "Secondary Interrupt Status 3 (ISR_S3)"

6.5.38 Secondary Interrupt Status 4 (ISR_S4_S)

Address: 0x1000_00D4
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S4	Same format as "Secondary Interrupt Status 4 (ISR_S4)"

6.5.39 Secondary Interrupt Status 5 (ISR_S5_S)

Address: 0x1000_00D4
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as Cold Reset)

Bit	Name	Description
31:0	ISR_S5	Same format as "Secondary Interrupt Status 5 (ISR_S5)"

6.6 QCU Registers

The QCU registers occupy the address space 0x1000_0800– 0x1000_0A40 in the memory of the ARXXXX. The ARXXXX has ten QCUs, numbered from 0 to 9.

Table 6-7. **QCU Registers**

Offset	Name	Description	Page
0x1000_0800 + (*Q* << 2)[1]	Q_TXDP	Transmit Queue Descriptor Pointer	page 77
0x1000_0840	Q_TXE	Transmit Queue Enable	page 78
0x1000_0880	Q_TXD	Transmit Queue Disable	page 78
0x1000_08C0 + (*Q* << 2)[1]	Q_CBRCFG	CBR Configuration	page 78
0x1000_0900 + (*Q* << 2)[1]	Q_RDYTIMECFG	ReadyTime Configuration	page 79
0x1000_0940	Q_ONESHOTARM_SC	OneShotArm Set Control	page 79
0x1000_0980	Q_ONESHOTARM_CC	OneShotArm Clear Control	page 79
0x1000_09C0 + (*Q* << 2)[1]	Q_MISC	Miscellaneous QCU Settings	page 80
0x1000_0A00 + (*Q* << 2)[1]	Q_STS	Miscellaneous QCU Status	page 82
0x1000_0A40	Q_RDYTIMESHDN	ReadyTimeShutdown Status	page 82

[1]The variable Q in the register addresses refers to the QCU number.

Beacon Handling

Table 6-8. **AP in a BSS: Sending Beacon and CAB**

<table>
<tr><th>QCU</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">QCU 9</td><td colspan="2">QCU 9 is used only for beacons
QCU 9 feeds into DCU 9, and is the only QCU to feed into DCU 9</td></tr>
<tr><td>For QCU 9</td><td>For DCU 9</td></tr>
<tr><td>1. Set FSP to DBA-gated (see bits [3:0] of “Misc. QCU Settings (Q_MISC)”).
2. Set the bit so the QCU sends beacons (Q_MISC bit [7]).
3. Set the bit to disable CBRExpired counter increment if the local queue has no frames (Q_MISC bit [5]).</td><td>1. Set the bit so DCU sends beacons (bit [16] of “Misc. DCU-Specific Settings (D_MISC)”).
2. Set the bit to enable global lockout (set D_MISC bits [18:17] to 0x2).
3. Set both CW_MIN and CW_MAX to zero (see “DCU-Specific IFS Settings (D_LCL_IFS)”).</td></tr>
<tr><td rowspan="3">QCU 8</td><td colspan="2">QCU 8 is used only for CAB (for a BSS, CAB is BCAST and MCAST frames)
QCU 8 feeds into DCU 8, and is the only QCU to feed into DCU 8</td></tr>
<tr><td>For QCU 8</td><td>For DCU 8</td></tr>
<tr><td>1. Set FSP to DBA-gate
2. Set the ReadyTimeEn bit and set the ReadyTimeDuration (RTD) to:
RTD = BeaconInterval – (SBA – DBA)
■ BeaconInterval is the interval between TBTTs
■ SBA is the amount of time before TBTT that SBA is generated
■ DBA is the amount of time before TBTT that DBA is generated
3. Set the bit to disable the CBRExpired counter increment if the beacon queue has no frames (bit [6] of “Misc. QCU Settings (Q_MISC)”).
4. Set the bit to disable the CBRExpired counter increment if the local queue has no frames (Q_MISC bit [5]).</td><td>1. Set the bit to enable global lockout.
2. Software tasks at SBA (all of these must occur before DBA):
■ Build beacon and pass it to QCU 9.
■ Build CAB and pass it to QCU 8.
■ Clear all Tx filter bits for DCUs 9 and 8.</td></tr>
</table>

Table 6-9. **STA in an IBSS: Sending Beacon and CAB**

QCU	Description	
QCU 9	QCU 9 is used only for beacons QCU 9 feeds into DCU 9, and is the only QCU to feed into DCU 9	
	For QCU 9	**For DCU 9**
	1. Set FSP to DBA-gated (Q_MISC bits [3:0]). 2. Set the bit so the QCU sends beacons (Q_MISC bit [7]).	1. Set DCU to send beacons (D_MISC bit [16]). 2. Set the bit to enable global lockout (set D_MISC bits [18:17] to 0x2). 3. Set both CW_MIN and CW_MAX to twice the usual CW_MIN value (refer to the 802.11 specifications).
QCU 8	QCU 8 is used only for CAB (for an IBSS, CAB is ATIMs followed by data frames requiring preceding ATIM reception) QCU 8 feeds into DCU 8, and is the only QCU to feed into DCU 8	
	For QCU 8	**For DCU 8**
	1. Set FSP to DBA-gate 2. Set the ReadyTimeEn bit and set the ReadyTimeDuration (RTD) to: RTD = $BeaconInterval - (SBA - DBA)$ 3. Set the bit to disable the CBRExpired counter increment if the beacon queue has no frames (bit [6] of "Misc. QCU Settings (Q_MISC)"). 4. Set the bit to disable the CBRExpired counter increment if the beacon queue has no frames (Q_MISC bit [6]). 5. Set the bit to disable the CBRExpired counter increment if the local queue has no frames (Q_MISC bit [5]). 6. Set the bit to clear TXE if ReadyTime expires (Q_MISC bit [9]).	1. Set the bit to enable global lockout. 2. Software tasks at SBA (all of these must occur before DBA): ■ Build beacon and pass it to QCU 9. ■ Build CAB and pass it to QCU 8. ■ Clear all Tx filter bits for DCUs 9 and 8.

6.6.1 Tx Queue Descriptor (Q_TXDP)

Address: 0x1000_0800 + (*Q* < 2)
Access: Read/Write
Cold Reset: (Undefined)
Warm Reset: (Unaffected)

Bit	Name	Description
31:2	TXDP	Tx descriptor pointer
1:0	RES	Reserved

6.6.2 Tx Queue Enable (Q_TXE)

Address: 0x1000_0840
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

NOTE: Writing a 1 in bit position *N* sets the TXE bit for QCU *N*. Writing a 0 in bit position *N* has no effect; in particular, it does not clear the TXE bit for the QCU.

Bit	Description
31:10	Reserved
9	Enable QCU 9
...	...
1	Enable QCU 1
0	Enable QCU 0

6.6.3 Tx Queue Disable (Q_TXD)

Address: 0x1000_0880
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

NOTE:
To stop transmission for QCU *Q*:

1. Write a 1 to QCU Q's TXD bit
2. Poll the "Tx Queue Enable (Q_TXE)" register until QCU *Q*'s TXE bit is clear
3. Poll QCU *Q*'s "Misc. QCU Status (Q_STS)" register until its pending frame count (Q_STS bits [1:0]) is zero
4. Write a 0 to QCU *Q*'s TXD bit

At this point, QCU *Q* has shut down and has no frames pending in its associated DCU.

Software must not write a 1 to a QCU's TXE bit when that QCU's TXD bit is set; an undefined operation will result. Software must ensure that it sets a QCU's TXE bit only when the QCU's TXD bit is clear. It is fine to write a 0 to TXE when TXD is set, but this has no effect on the QCU.

Bit	Description
31:10	Reserved
9	Disable QCU 9
...	...
1	Disable QCU 1
0	Disable QCU 0

6.6.4 CBR Configuration (Q_CBRCFG)

Address: 0x1000_08C0 + (Q < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

Bit	Name	Description
31:24	CBR_OVF_THRESH	CBR overflow threshold
23:0	CBR_INTV	CBR interval in µs

6.6.5 ReadyTime Configuration (Q_RDYTIMECFG)

Address: 0x1000_0900 + (*Q* < 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

Bit	Name	Description	
31:25	RES	Reserved	
24	RDYTIME_EN	ReadyTime enable	
		0	Disable ReadyTime use
		1	Enable ReadyTime use
23:0	RDYTIME_DUR	ReadyTime duration in µs	

6.6.6 OneShotArm Set Control (Q_ONESHOTARM_SC)

Address: 0x1000_0940
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

NOTE: A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Description	
31:10	Reserved	
9	0	No effect
	1	Set OneShot arm bit for QCU 9
...	...	
1	0	No effect
	1	Set OneShot arm bit for QCU 1
0	0	No effect
	1	Clears the ReadyTime shutdown status bit

6.6.7 OneShotArm Clear Control (Q_ONESHOTARM_CC)

Address: 0x1000_0980
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

NOTE: A read to this register returns the current state of all OneShotArm bits (QCU *Q*'s OneShotArm bit is returned in bit position *Q*).

Bit	Description	
31:10	Reserved	
9	0	No effect
	1	Clear OneShot arm bit for QCU 9
...	...	
1	0	No effect
	1	Clear OneShot arm bit for QCU 1
0	0	No effect
	1	Clear OneShot arm bit for QCU 0

6.6.8 Misc. QCU Settings (Q_MISC)

Address: 0x1000_09C0 + (*Q* < 2)
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Same as cold reset)

Bit	Name	Reset	Description	
31:12	RES	0x0	Reserved	
11	QCU_FR_ABORT_REQ_EN	0x1	DCU frame early termination request control	
			0	Never request early frame termination. Once a frame enters the DCU, it will remain active until its normal retry count has been reached or the frame succeeds.
			1	Allow this QCU to request early frame termination. When requested, the DCU attempts to complete processing the frame more quickly than it normally would.
10	CBR_EXP_CNT_CLR_EN	0x0	CBR expired counter force-clear control. Write-only (always reads as zero). Write of:	
			0	No effect
			1	Resets the CBR expired counter to zero
9	TXE_CLR_ON_CBR_END	0x0	ReadyTime expiration and VEOL handling policy	
			0	On expiration of ReadyTime or on VEOL, the TXE bit is not cleared. Only reaching the physical end-of-queue (that is, a NULL LinkPtr) will clear TXE
			1	The TXE bit is cleared on expiration of ReadyTime, on VEOL, and on reaching the physical end-of-queue
8	CBR_EXP_INC_LIMIT	0x0	CBR expired counter limit enable	
			0	The maximum CBR expired counter value is 255, but a CBROVF interrupt is generated when the counter reaches the value set in the CBR overflow threshold field of the "CBR Configuration (Q_CBRCFG)" register.
			1	The maximum CBR expired counter is limited to the value of the CBR overflow threshold field of the "CBR Configuration (Q_CBRCFG)" register. Note that in addition to limiting the maximum CBR expired counter to this value, a CBROVF interrupt is also generated when the CBR expired counter reaches the CBR overflow threshold.
7	QCU_IS_BCN	0x0	Beacon use indication. Indicates whether the QCU is being used for beacons	
			0	QCU is being used for non-beacon frames only
			1	QCU is being used for beacon frames (and possibly for non-beacon frames)
6	CBR_EXP_INC_DIS_NOBCNFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the QCU marked as being used for beacon transmission (i.e., the QCU that has bit [7] set in its "Misc. QCU Settings (Q_MISC)" register) contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the beacon queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the beacon queue is valid (the beacon queue is valid whenever its TXE is asserted)

Bit	Name	Reset	Description	
5	CBR_EXP_INC _DIS_NOFR	0x0	Disable the CBR expired counter increment if the frame scheduling trigger occurs and the queue contains no frames	
			0	Increment the CBR expired counter each time the frame scheduling trigger occurs, regardless of whether the queue contains frames
			1	Increment the CBR expired counter only when both the frame scheduling trigger occurs and the queue is valid (the queue is valid whenever TXE is asserted)
4	ONESHOT_EN	0x0	OneShot enable	
			0	Disable OneShot function
			1	Enable OneShot function Note that OneShot must not be enabled when the QCU is set to an ASAP frame scheduling policy.
3:0	FSP	0x0	Frame scheduling policy setting	
			0	ASAP The QCU is enabled continuously.
			1	CBR The QCU is enabled under control of the settings in the "CBR Configuration (Q_CBRCFG)" register.
			2	DBA-gated The QCU will be enabled at each occurrence of a DMA beacon alert.
			3	TIM-gated The QCU will be enabled whenever: ■ In STA mode, the PCU indicates that a beacon frame has been received with the local STA's bit set in the TIM element ■ In IBSS mode, the PCU indicates that an ATIM frame has been received
			4	Beacon-sent-gated The QCU will be enabled when the DCU that is marked as being used for beacon transmission (see bit [16] of the "Misc. DCU-Specific Settings (D_MISC)" register) indicates that it has sent the beacon frame on the air
			5	Beacon-received-gated The QCU will be enabled when the PCU indicates that it has received a beacon.
			6	HCF Poll gated The QCU will be enabled whenever the Rx HCF poll event occurs; the signals come from the PCU when a directed HCF poll frame type is received with valid FCS.
			15:7	Reserved

6.6.9 Misc. QCU Status (Q_STS)

Address: 0x1000_0A00 + ($Q < 2$)
Access: Read-Only
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

Bit	Description
31:16	Reserved
15:8	Current value of the CBR expired counter
7:2	Reserved
1:0	Pending frame count Indicates the number of frames this QCU presently has pending in its associated DCU.

6.6.10 ReadyTimeShutdown Status (Q_RDYTIMESHDN)

Address: 0x1000_0A40
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Same as cold reset)

<table>
<tr><th>Bit</th><th colspan="2">Description</th></tr>
<tr><td>31:10</td><td colspan="2">Reserved</td></tr>
<tr><td>9</td><td colspan="2">ReadyTimeShutdown status for QCU 9</td></tr>
<tr><td>...</td><td colspan="2">...</td></tr>
<tr><td>1</td><td colspan="2">ReadyTimeShutdown status for QCU 1</td></tr>
<tr><td rowspan="3">0</td><td colspan="2">ReadyTimeShutdown status for QCU 0
On read, returns ReadyTimeShutdown indication. Write of:</td></tr>
<tr><td>0</td><td>No effect</td></tr>
<tr><td>1</td><td>Clears the ReadyTimeShutdown status bit</td></tr>
</table>

6.7 DCU Registers

The DCU registers occupy the address space 0x1000_1000– 0x1000_12F0 in the memory of the ARXXXX. The ARXXXX has ten DCUs, numbered from 0 to 9.

Table 6-8. **DCU Registers**

Offset	Name	Description	Page
0x1000_1000 + (*D* << 2)[1]	D_QCUMASK	QCU Mask	page 83
0x1000_1040 + (*D* << 2)[1]	D_LCL_IFS	DCU-Specific IFS Settings	page 84
0x1000_1080 + (*D* << 2)[1]	D_RETRY_LIMIT	Retry Limits	page 84
0x1000_10C0 + (*D* << 2)[1]	D_CHNTIME	ChannelTime Settings	page 85
0x1000_1100 + (*D* << 2)[1]	D_MISC	Miscellaneous DCU-Specific Settings	page 85
0x1000_1030	D_GBL_IFS_SIFS	DCU-Global IFS Settings: SIFS Duration	page 87
0x1000_1070	D_GBL_IFS_SLOT	DCU-Global IFS Settings: Slot Duration	page 88
0x1000_10B0	D_GBL_IFS_EIFS	DCU-Global IFS Settings: EIFS Duration	page 88
0x1000_10F0	D_GBL_IFS_MISC	DCU-Global IFS Settings: Misc. Parameters	page 88
0x1000_1270	D_TXPSE	DCU Transmit Pause Control/Status	page 89
0x1000_12F0	D_TXSLOTMASK	DCU Transmission Slot Mask	page 89
(Varies)	D_TXBLK	DCU Transmit Filter Bits	page 91

[1]The variable *D* in the register addresses refers to the DCU number.

6.7.1 QCU Mask (D_QCUMASK)

Address: 0x1000 + (*D* << 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Unaffected)

NOTE: To achieve lowest power consumption, software should set this register to 0x0 for all DCUs that are not in use. The hardware detects that the QCU mask is set to zero and shuts down certain logic in response, helping to save power.

Bit	Name	Description
31:10	RES	Reserved
9:0	QCU_MASK	QCU mask Setting bit *Q* means that QCU *Q* is associated with (i.e., feeds into) this DCU. These register have reset values which corresponding to a 1 to 1 mapping between QCUs and DCUs. A register offset of 0x1000 maps to 0x1, 0x1004 maps to 0x2, 0x1008 maps to 0x4, etc.

6.7.2 DCU-Specific IFS Settings (D_LCL_IFS)

Address: 0x1000_1040 + (*D* << 2)
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Unaffected)

Bit	Name	Reset	Description
When Long AIFS is 0:			
31:28	RES	0x0	Reserved
27:20	DATA_AIFS_D[7:0]	0x2	AIFS value, in slots beyond SIFS For example, a setting of 2 (the reset value) means AIFS is equal to DIFS. **NOTE:** Although this field is 17 bits wide (including the 9 MSBs accessed using the long AIFS field), the maximum supported AIFS value is 0x1FFFC. Setting the AIFS value to 0x1FFFD, 0x1FFFE, or 0x1FFFF does not work correctly and causes the DCU to hang.
19:10	DATA_CW_MAX	0x3FF	CW_MAX value; must be equal to a power of 2, minus 1
9:0	DATA_CW_MIN	0xF	CW_MIN value; must be equal to a power of 2, minus 1
When Long AIFS is 1:			
31:29	RES	0x0	Reserved
28	LONG_AIFS [DCU_IDX_D]	0x0	Long AIFS bit; used to read or write to the nine MSBs of the AIFS value
27:9	RES	0x0	Reserved
8:0	DATA_AIFS_D[16:8]	0x2	Upper nine bits of the AIFS value (see bits [27:20] listed in this register)

6.7.3 Retry Limits (D_RETRY_LIMIT)

Address: 0x1000_1080 + (*D* << 2)
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Unaffected)

Bit	Name	Reset	Description
31:20	RES	0x20	Reserved
19:14	SDFL	0x20	STA data failure limit Specifies the number of times a frame's data exchange may fail before CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
13:8	SRFL	0x20	STA RTS failure limit Specifies the number of times a frame's RTS exchange may fail before the CW is reset to CW_MIN. Note: A value of 0x0 is unsupported.
7:4	RES	0x0	Reserved
3:0	FRFL	0x4	Frame RTS failure limit Specifies the number of times a frame's RTS exchange may fail before the current transmission series is terminated. A frame's RTS exchange fails if RTS is enabled for the frame, but when the MAC sends the RTS on the air, no CTS is received. Note: A value of 0x0 is unsupported.

6.7.4 ChannelTime Settings (D_CHNTIME)

Address: 0x1000_10C0 + (*D* << 2)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Unaffected)

Bit	Name	Description	
31:21	RES	Reserved	
20	CHANNEL_TIME_EN	ChannelTime enable	
		0	Disable ChannelTime function
		1	Enable ChannelTime function
19:0	DATA_CT_MMR	ChannelTime duration in µs	

6.7.5 Misc. DCU-Specific Settings (D_MISC)

Address: 0x1000_1100 + (*D* << 2)
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Unaffected)

Bit	Name	Reset	Description	
31:24	RES	0x0	Reserved	
23	RETRY_ON_BLOWN_IFS_EN	0x0	Blown IFS handling policy This setting controls how the DCU handles the case in which the DMA of a frame takes so long that the IFS spacing is met before the frame trigger level is reached.	
			0	Send the frame on the air anyway (i.e., ignore the IFS violation). This will cause the frame to be sent on the air at a time that is later than called for in the 802.11 spec.
			1	Do not send the frame on the air. Instead, act as if the frame had been sent on the air but failed and initiate the retry procedure. A retry will be charged against the frame. If more retries are permitted, the frame will be retried. If the retry limit has been reached, the frame will fail.
22	VIRT_COLL_CW_INC_EN	0x0	Virtual collision CW increment policy	
			0	Virtual collisions do not increment (advance) the frame’s contention window (CW)
			1	Virtual collisions do increment the frame’s contention window (CW)
21	POST_BKOFF_SKIP	0x0	Post-frame backoff disable	
			0	DCU performs a backoff after each frame finishes
			1	DCU skips the post-frame backoff (or, equivalently, acts as if it always selects a post-frame backoff count of zero)
20	SEQNUM_FREEZE	0x0	Sequence number increment disable	
			0	Allow the DCU to use a normal sequence number progression (the DCU increments the sequence number for each new frame)
			1	Force the sequence number to be frozen at its current value

Bit	Name	Reset	Description	
19	DCU_ARB_LOCKOUT_IGNORE	0x0	DCU arbiter lockout ignore control	
			0	Obey DCU arbiter lockouts from higher-priority DCUs
			1	Ignore DCU arbiter lockouts from higher-priority DCUs (i.e., allow the current DCU to arbitrate for access to the PCU even if one or more higher-priority DCUs is asserting a DCU arbiter lockout)
18:17	DCU_ARB_LOCKOUT_IF_EN	0x0	DCU arbiter lockout control	
			0	No lockout. Allows lower-priority DCUs to arbitrate for access to the PCU concurrently with this DCU.
			1	Intra-frame lockout only. Forces all lower-priority DCUs to defer arbitrating for access to the PCU while the current DCU is either arbitrating for access to the PCU or performing an intra-frame backoff.
			2	Global lockout. Forces all lower-priority DCUs to defer arbitrating for access to the PCU whenever: ■ At least one of the QCUs that feed into the current DCU has a frame ready ■ The current DCU is actively processing a frame (i.e., is not idle). This includes arbitrating for access to the PCU, performing an intra-frame or post-frame backoff, DMA'ing frame data to the PCU, or waiting for the PCU to complete the frame.
			3	Reserved
16	DCU_IS_BRN	0x0	Beacon use indication Indicates whether the DCU is being used for beacons.	
			0	DCU is being used for non-beacon frames only
			1	DCU is being used for beacon frames only
15:14	VIRT_COLL_POLICY	0x0	Virtual collision handling policy	
			0	Default handling. A virtual collision is processed as a collision on the air except that the retry count for the frame is not incremented (i.e., just perform the backoff).
			1	Ignore. Virtual collisions are ignored (i.e., the DCU immediately rearbitrates for access to the PCU without doing a backoff or incrementing the retry count).
			3:2	Reserved
13	RES	0x0	Reserved	
12	MEM_RD_DATA_PF	0x1	Backoff persistence factor setting	
			0	New CW equals old CW
			1	Use binary-exponential CW progression
11:10	RES	0x0	Reserved	
9	FRAG_BURST_BKOFF_EN	0x0	Fragment burst backoff policy This bit controls whether the DCU performs a backoff after each transmission of a fragment (i.e., a frame with the MoreFrag bit set in the frame control field).	
			0	The DCU handles fragment bursts normally
			1	Modified handling. The DCU performs a backoff after all fragments, even those transmitted successfully.

Bit	Name	Reset	Description
8	FRAG_BURST _WAIT_QCU_EN	0x0	Fragment burst frame starvation handling policy This bit controls the DCU operation when the DCU is in the middle of a fragment burst and finds that the QCU sourcing the fragments does not have the next fragment available. 0 — The DCU terminates the fragment burst. Note that when this occurs, the remaining fragments (when the QCU eventually has them available) will be sent as a separate fragment burst with a different sequence number. 1 — The DCU waits for the QCU to have the next fragment available. While doing so, all other DCUs will be unable to transmit frames.
7	TS_END_DIS	0x0	End of transmission series CW reset policy This bit controls only whether the contention window is reset when transitioning from one transmission series to the next within a single frame. The CW is reset per the 802.11 spec when the entire frame attempt terminates (because the frame was sent successfully or because all transmission series failed). 0 — Reset the CW to CW_MIN at the end of each intraframe transmission series 1 — Do not reset the CW at the end of each intraframe transmission series
6	SFC_RST_AT _TS_END_EN	0x0	End of transmission series station RTS/data failure count reset policy Note that this bit controls only whether the two STA failure counts are reset when transitioning from one transmission series to the next within a single frame. The counts are reset per the 802.11 spec when the entire frame attempt terminates (either because the frame was sent successfully or because all transmission series failed). 0 — Do not reset the station RTS failure count or the STA data failure count at the end of each transmission series 1 — Reset both the station RTS failure count and the STA data failure count at the end of each transmission series
5:0	DATA _BKOFF_THRESH	0x2	Backoff threshold setting Determines the backoff count at which the DCU will initiate arbitration for access to the PCU and commit to sending the frame.

6.7.6 DCU-Global IFS Settings: SIFS Duration (D_GBL_IFS_SIFS)

Address: 0x1000_1030
Access: Read/Write
Cold Reset: 640 (16 µs at 40 MHz)
Warm Reset: (Unaffected)

Bit	Name	Description
31:16	RES	Reserved
15:0	SIFS_DUR	SIFS duration in core clocks (40 MHz in non-Turbo mode, 80 MHz in Turbo mode)

6.7.7 DCU-Global IFS Settings: Slot Duration (D_GBL_IFS_SLOT)

Address: 0x1000_1070
Access: Read/Write
Cold Reset: 360 (9 µs at 40 MHz)
Warm Reset: (Unaffected)

Bit	Name	Description
31:16	RES	Reserved
15:0	SLOT_DUR	Slot duration in core clocks (40 MHz in non-Turbo mode, 80 MHz in Turbo mode)

6.7.8 DCU-Global IFS Settings: EIFS Duration (D_GBL_IFS_EIFS)

Address: 0x1000_10B0
Access: Read/Write
Cold Reset: 3480 (87 µs at 40 MHz)
Warm Reset: (Unaffected)

Bit	Name	Description
31:16	RES	Reserved
15:0	EIFS_DUR	EIFS duration in core clocks (40 MHz in non-Turbo mode, 80 MHz in Turbo mode)

6.7.9 DCU-Global IFS Settings: Misc. Parameters (D_GBL_IFS_MISC)

Address: 0x1000_10F0
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Unaffected)

<table>
<tr><th>Bit</th><th>Name</th><th>Reset</th><th colspan="2">Description</th></tr>
<tr><td>31:29</td><td>RES</td><td>0x0</td><td colspan="2">Reserved</td></tr>
<tr><td>28</td><td>IGNORE
_BACKOFF</td><td>0x0</td><td colspan="2">Ignore back off
Allows the DCU to ignore backoff as well as EIFS; it should be set during fast channel change to guarantee low latency to flush the Tx pipe.</td></tr>
<tr><td>27</td><td>CHAN_SLOT
_ALWAYS</td><td>0x0</td><td colspan="2">Force transmission always on slot boundaries
When bits [26:25] of this register are non-zero, the MAC transmits on slot boundaries as required by the 802.11 spec. When bits [26:25] are not 0x0 and this bit is non-zero, the MAC always transmits on slot boundaries.</td></tr>
<tr><td>26:25</td><td>CHAN_SLOT
_WIN_DUR</td><td>0x0</td><td colspan="2">Slot transmission window length
Specifies the number of core clocks after a slot boundary during which the MAC is permitted to send a frame. Specified in units of 8 core clocks, with the value 0x0 being special. If set to a value of 0x0 (the reset value), the MAC is permitted to send at any point in the slot.</td></tr>
<tr><td rowspan="3">24</td><td rowspan="3">LFSR_SLICE
_RANDOM_DIS</td><td rowspan="3">0x0</td><td colspan="2">Random LFSR slice selection disable</td></tr>
<tr><td>0</td><td>Allow the IFS logic to randomly generate the LFSR slice select value (see bits [2:0] of this register).</td></tr>
<tr><td>1</td><td>Disable random LFSR slice selection and use the value of the LFSR slice select field (bits [2:0] of this register) instead</td></tr>
</table>

Bit	Name	Reset	Description
23:3	RES	0x0	Reserved
2:0	LFSR_SLICE_SEL	0x0	LFSR slice select Determines which slice of the internal LFSR will generate the random sequence used to determine backoff counts in the PCU's DCUs and scrambler seeds. This allows different STAs to contain different LFSR slice values (e.g., by using bits from the MAC address) to minimize random sequence correlations among STAs in the same BSS/IBSS. **NOTE:** This field affects the MAC only when the random LFSR slice selection disable bit (bit [24] of this register) is set. When random LFSR slice selection is enabled (the default), this field is ignored.

6.7.10 DCU Tx Pause Control/Status (D_TXPSE)

Address: 0x1000_1270
Access: Read/Write
Cold Reset: (See field descriptions)
Warm Reset: (Unaffected)

Bit	Name	Reset	Description	
31:17	RES	0x0	Reserved	
16	TX_PAUSED	0x1	Tx pause status	
			0	Tx pause request has not yet taken effect, so some DCUs for which a transmission pause request has been issued using bits [9:0] of this register are still transmitting and have not paused.
			1	All DCUs for which a transmission pause request has been issued via bits [9:0] of this register, if any, have paused their transmissions. Note that if no transmission pause request is pending (i.e., bits [9:0] of this register are all set to 0), then this Tx pause status bit will be set to one.
15:10	RES	0x0	Reserved	
9:0	DCU_REG_TXPSE	0x0	Request that some subset of the DCUs pause transmission. For bit *D* of this field ($9 \geq D \geq 0$):	
			0	Allow DCU *D* to continue to transmit normally
			1	Request that DCU *D* pause transmission as soon as it is able

6.7.11 DCU Transmission Slot Mask (D_TXSLOTMASK)

Address: 0x1000_12F0
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Unaffected)

NOTE: When bits [26:25] of the "DCU-Global IFS Settings: Misc. Parameters (D_GBL_IFS_MISC)" register are non-zero, D_TXSLOTMASK controls the slots DCUs can start frame transmission on. The slot occurring coincident with SIFS elapsing is slot 0. Slot numbers increase thereafter, whether the channel was idle or busy during the slot. If bits [26:25] of D_GBL_IFS_MISC are zero, this register has no effect.

Bit	Description
31:16	Reserved

Bit	Description	
15	Specifies whether transmission may start on slot numbers that are congruent to 15 (mod 16)	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots
...	...	
1	Specifies whether transmission may start on slot numbers that are congruent to 1 (mod 16)	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots
0	Specifies whether transmission may start on slot numbers that are congruent to 0 (mod 16)	
	0	Transmission may start on such slots
	1	Transmission may not start on such slots

6.7.12 DCU Tx Filter Bits (D_TXBLK)

Offset: Varies (see Table 6-9)
Access: Read/Write
Cold Reset: 0x0
Warm Reset: (Unaffected)

Each DCU has 128 Tx filter bits, for a total of 10 * 128=1280 Tx filter bits for all ten DCUs.

For reads of the Tx filter bits, the 1280 bits are accessed via reads within a range of 64 32-bit register locations.

For writes of the Tx filter bits, only three of the 64 register locations are used. One location allows specific bits of a specific DCU's Tx filter bits to be set or cleared. Two other locations allow all 128 Tx filter bits for any subset of the ten DCUs to be set or cleared atomically.

For both reads and writes, the offset issued by the host is mapped to one of the 64 register locations. The 6-bit internal address resulting from mapping is called MMR_ADDR, and its value controls what portion of the Tx filter bits is affected by the host's register read or write. In general, the address offset that maps to the internal MMR_ADDR is given by the equation:

> Address offset = 0x1038 +
> ((mmr_addr & 0x1f) << 6) +
> ((mmr_addr & 0x20) >> 3)

Thus the proper address offset can be determined from the desired MMR_ADDR (see Table 6-9).

Table 6-9. **MMR_ADDR and Address Offset**

Table 6-9. **MMR_ADDR and Address Offset**

MMR_ADDR	Address Offset
0	0x1038
1	0x1078
2	0x10B8
3	0x10F8
4	0x1138
5	0x1178
6	0x11B8
7	0x11F8
8	0x1238
9	0x1278
10	0x12B8
11	0x12F8
12	0x1338
13	0x1378
14	0x13B8
15	0x13F8
16	0x1438
17	0x1478
18	0x14B8
19	0x14F8
20	0x1538
21	0x1578
22	0x15B8
23	0x15F8
24	0x1638
25	0x1678
26	0x16B8
27	0x16F8
28	0x1738
29	0x1778
30	0x17B8
31	0x17F8
...	...
48	0x143C
49	0x147C

Writes

Only three register locations (MMR_ADDR values) are supported for writes. Writes to other values yield undefined results and may corrupt Tx filter bits.

Table 6-10. **MMR_ADDR Usage for Tx Filter Bits (Write Data)**

MMR_ADDR	Description		
49	Sets all 128 filter bits for each DCU that has a 1 in bits [9:0] of the write data (e.g., a write of 0x5 to address 49 causes all 128 filter bits for DCUs 0 and 2 to be set)		
48	Clears all 128 filter bits for each DCU that has a 1 in bits [9:0] of the write data (e.g., a write of 0x5 to address 48 causes all 128 filter bits for DCUs 0 and 2 to be cleared)		
0	Allows individual bits of a particular DCU's 128 Tx filter bits to modify. The write data determines which bits are affected and what operation is performed. The write data is split into several fields:		
	31:28	Reserved	
	27:24	Command; determines what operation will be performed on the selected filter bits:	
		0	Clear the selected bits
		1	Set the selected bits
		15:2	Reserved
	23:20	DCU number; determines which DCU's Tx filter bits are affected by writes. Setting this field to a value of D ($9 \geq D \geq 0$) causes DCU D's Tx filter bits to be affected by the write.	
	19:16	Slice number; selects a 16-bit bitslice from the selected DCU's 128 affected Tx filter bits:	
		0	Filter bits [15:0] are affected
		1	Filter bits [31:16] are affected
		...	...
		7	Filter bits [127:112] are affected
		15:8	Reserved
	15:0	Bitmask; controls which bits within the selected bitslice are affected. Bit N ($15 \geq N \geq 0$) of the bitmask affects bit N of the selected bitslice (see examples):	
		0	Bit N remains unchanged
		1	Bit N of the selected bitslice is modified per the command field (bits [27:24])
		Example Write Data	**Example Effect**
		0x130404	Clears bits [50] and [58] of DCU 1's Tx filter bits
		0x00978001	Clears bits [127] and [112] of DCU 9's Tx filter bits

Reads

Table 6-11. **MMR_ADDR Usage for Tx Filter Bits (Read Data)**

MMR_ADDR	Description
49:48	No effect
39:36	Returns filter bits for DCU 9, bits [31:0] – [127:96]
...	...
7:4	Returns filter bits for DCU 1, bits [31:0] – [127:96]
3	Returns filter bits for DCU 0, bits [127:96]
2	Returns filter bits for DCU 0, bits [95:64]
1	Returns filter bits for DCU 0, bits [63:32]
0	Returns filter bits for DCU 0, bits [31:0]

EEPROM Interface Registers

This EEPROM registers access the external EEPROM. Upon power reset, a state machine inside the host interface reads the EEPROM and writes registers within the ARXXXX. The EEPROM map is shown in Figure 6-1:

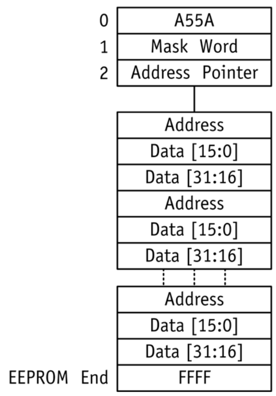


Figure 6-1. **EEPROM Address Map**

Each EEPROM location is 16 bits wide. As shown in Figure 6-1, the first location must contain the 16-bit word A55A, indicating that the EEPROM is valid. If the first location is not this value, then the state machine assumes the EEPROM contents have been corrupted and immediately stops running.

The next EEPROM location contains the mask word as described. Location 2 contains an address pointer to the next valid data segment. Each data segment consists of three locations: a 16-bit address location and two locations for the 32-bit write data as shown in Figure 6-1. The state machine reads each data segment and writes to the corresponding ARXXXX register. The state machine stops when it comes to an address equal to FFFF.

6.8 Host Interface Registers

Table 6-12. **Host Interface Registers**

Offset	Name	Description	Page
0x1000_4000	H_RC	Reset the MAC AHB/APB Interface	page 94
0x1000_401C	H_EEPROM_CTRL	EEPROM Control	page 94
0x1000_4020	H_SREV_ID	MAC Silicon Revision ID	page 94
0x1000_4024	AHB_MODE	AHB Mode	page 95
0x1000_4028	H_INTR_CAUSE_CLR	Interrupt Cause Clear	page 96
0x1000_4028	H_INTR_SYNC_CAUS	Synchronous Interrupt Cause	page 96
0x1000_402C	H_INTR_SYNC_ENAB	Synchronous Interrupt Enable	page 97
0x1000_4030	H_INTR_ASYN_MASK	Asynchronous Interrupt Mask	page 97
0x1000_4034	H_INTR_SYN_MASK	Synchronous Interrupt Mask	page 97
0x1000_4038	H_INTR_ASYN_CAUS	Asynchronous Interrupt Cause	page 97
0x1000_403C	H_INTR_ASYN_ENAB	Asynchronous Interrupt Enable	page 97
0x1000_4048	H_GPIO_IN_OUT	GPIO Input and Output	page 98
0x1000_404C	H_GPIO_OE_BITS	GPIO Output Enable Bits	page 98
0x1000_4050	H_GPIO_IRQ_POLAR	GPIO Interrupt Polarity	page 99
0x1000_4054	H_GP_INPT_EN_VAL	GPIO Input Enable and Value	page 99
0x1000_4058	H_GP_INPT_MUX1	GPIO Input MUX1	page 99
0x1000_405C	H_GP_INPT_MUX2	GPIO Input MUX2	page 100
0x1000_4060	H_GP_OUTPT_MUX1	GPIO Output MUX1	page 100
0x1000_4064	H_GP_OUTPT_MUX2	GPIO Output MUX2	page 100
0x1000_406C	H_INPUT_STATE	Input Values	page 101
0x1000_407C	H_EEP_STS_DATA	EEPROM Status and Read Data	page 102
0x1000_4084	H_RFSILENT	RFsilent-Related Registers	page 102
0x1000_4088	H_GPIO_PDPU	GPIO Pull-Up/Pull-Down	page 103
0x1000_408C	H_GPIO_DS	GPIO Drive Strength	page 103
0x1000_40B8	MAC_AHB_BURST_EN	AHB Burst Mode	page 104

6.8.1 Reset the MAC AHB/APB Interface (H_RC)

Address: 0x1000_4000
Access: Read/Write
Reset Value: 0000_0000

Bit	Description	
31:2	Reserved	
1	0	Normal MAC APB interface operation
	1	Hold MAC APB interface in reset
0	0	Normal MAC AHB interface operation
	1	Hold MAC AHB interface in reset

6.8.2 EEPROM Control (H_EEPROM_CTRL)

Address: 0x1000_401C
Access: Read/Write
Reset Value: 0000_00FC

Bit	Description	
31	LARGE_SIZE_EEPROM. Indicates that the size of the connected EEPROM is bigger than 16 Kbits.	
30:26	Reserved	
25:10	EEPROM protect mask	
9	EEPROM is corrupt	
8	EEPROM not present	
7:2	CLKDIV value for the APB EEPROM module	
1	0	Normal operation of the APB EEPROM module
	1	Reserved
0	0	Normal operation of the APB EEPROM module
	1	Reserved

6.8.3 MAC Silicon Revision ID (H_SREV_ID)

Address: 0x1000_4020
Access: Read-Only
Reset Value: 000C_12FF

Bit	Description	
31:18	3	Version
17:12	1	Type
11:8	2	Revision
7:0	255	Old revision

6.8.4 AHB Mode (AHB_MODE)

Address: 0x1000_4024
Access: Read-Only

This register is used to set the parameters for AHB mode.

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Type</th><th>Reset</th><th colspan="2">Description</th></tr>
<tr><td>31:9</td><td>RES</td><td>R</td><td>0x0</td><td colspan="2">Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>8</td><td>AGG_DMA_EN</td><td>R/W</td><td>0x0</td><td colspan="2">Enables enhanced DMA function for aggregation</td></tr>
<tr><td>7:6</td><td>RES</td><td>R</td><td>0x0</td><td colspan="2">Reserved. Must be written with zero. Contains zeros when read.</td></tr>
<tr><td>5</td><td>AHB_TRAIL_
OVERRIDE</td><td>R/W</td><td>0x0</td><td colspan="2">AHB Override</td></tr>
<tr><td rowspan="5">4:3</td><td rowspan="5">PAGE_SIZE</td><td rowspan="5">R/W</td><td rowspan="5">0x3</td><td colspan="2">Page size</td></tr>
<tr><td>0</td><td>1 Kbytes</td></tr>
<tr><td>1</td><td>2 Kbytes</td></tr>
<tr><td>2</td><td>4 Kbytes</td></tr>
<tr><td>3</td><td>4 Kbytes</td></tr>
<tr><td rowspan="5">2:1</td><td rowspan="5">READ_MODE</td><td rowspan="5">R/W</td><td rowspan="5">0x3</td><td colspan="2">AHB read mode</td></tr>
<tr><td>0</td><td>Exact read mode</td></tr>
<tr><td>1</td><td>CacheLine read mode</td></tr>
<tr><td>2</td><td>PreFetch read mode</td></tr>
<tr><td>3</td><td>PreFetch read mode</td></tr>
<tr><td>0</td><td>WRITE_MODE</td><td>R/W</td><td>0x1</td><td colspan="2">AHB write mode</td></tr>
</table>

Table 6-13 describes all of the signals capable of generating a system interrupt and lists their corresponding bits. The bits are the same for synchronous as well as asynchronous interrupts.

Table 6-13. **System Interrupt Registers: Bit Descriptions**

Bit	Name	Description
31:18	RES	Reserved
17	MAC_SLEEP_ACCESS	Software is trying to access a register within the MAC while it is asleep
16	MAC_ASLEEP	The MAC has gone to sleep
15	MAC_AWAKE	The MAC has become awake
14	PM_ACCESS	The AHB master is requesting that a DMA transfer to the core while it is asleep
13	LOCAL_TIMEOUT	A local bus timeout has occurred
12:4	RES	Reserved
3	APB_TIMEOUT	No response from one of the ARXXXX modules within the programmed timeout period during a register access
2	EEPROM_ILLEGAL_ACCESS	Software attempted to either access a protected area within the EEPROM, or access the EEPROM while it is busy or absent
1	MAC_IRQ	The MAC has requested an interrupt
0	RTC_IRQ	The RTC is in shutdown state

6.8.5 Interrupt Cause Clear (H_INTR_CAUSE_CLR)

Address: 0x1000_4028
Access: Write-Only
Reset Value: 0000_0000

Bit	Description
31:0	Writing a 1 to any bit in this register clears the corresponding bit in the "Synchronous Interrupt Cause (H_INTR_SYNC_CAUS)" register. See Table 6-13 for bit descriptions.

6.8.6 Synchronous Interrupt Cause (H_INTR_SYNC_CAUS)

Address: 0x1000_4028
Access: Read-Only
Reset Value: 0000_0000

Bit	Description
31:0	Setting any bit in this register indicates that the corresponding interrupt has been triggered in synchronous mode; for any bit to be to set in this register, the corresponding bit in the "Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)" register must also be set. See Table 6-13 for bit descriptions.

6.8.7 Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)

Address: 0x1000_402C
Access: Read/Write
Reset Value: 0000_0000

Bit	Description
31:0	Setting any bit in this register allows the corresponding interrupt signal to set its corresponding bit in the "Synchronous Interrupt Cause (H_INTR_SYNC_CAUS)" register. See Table 6-13 for bit descriptions.

6.8.8 Asynchronous Interrupt Mask (H_INTR_ASYN_MASK)

Address: 0x1000_4030
Access: Read/Write
Reset Value: 0000_0002

Bit	Description
31:0	Setting any bit in this register allows the corresponding interrupt signal to trigger an interrupt provided that the corresponding "Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)" register bit is set. Note that for this register bit to be set, the corresponding "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" register bit must also be set by software. See Table 6-13 for bit descriptions.

6.8.9 Synchronous Interrupt Mask (H_INTR_SYN_MASK)

Address: 0x1000_4034
Access: Read/Write
Reset Value: 0000_0000

Bit	Description
31:0	Setting any bit in this register allows the corresponding interrupt signal to trigger an interrupt provided that the corresponding "Synchronous Interrupt Cause (H_INTR_SYNC_CAUS)" register bit is set. Note that for this register bit to be set, the corresponding "Synchronous Interrupt Enable (H_INTR_SYNC_ENAB)" register bit must also be set by software. See Table 6-13 for bit descriptions.

6.8.10 Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)

Address: 0x1000_4038
Access: Read-Only
Reset Value: 0000_0000

Bit	Description
31:0	Setting any bit in this register indicates that the corresponding interrupt has been triggered in asynchronous mode. For any bit to be to set in this register, the corresponding bit in the "Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)" register must also be set. See Table 6-13 for bit descriptions.

6.8.11 Asynchronous Interrupt Enable (H_INTR_ASYN_ENAB)

Address: 0x1000_403C
Access: Read/Write
Reset Value: 0000_0002

Bit	Description
31:0	Any bit set to 1 in this register indicates that the corresponding interrupt signal to set its corresponding bit in the "Asynchronous Interrupt Cause (H_INTR_ASYN_CAUS)" register. See Table 6-13 for bit descriptions.

6.8.12 GPIO Input and Output (H_GPIO_IN_OUT)

Address: 0x1000_4048
Access: See field description
Reset Value: 000F_8C00

Bit	Bit Name	Type	Reset	Description
31:16	GPI	R	0x0	Actual Value of each GPIO signal
15:0	GPO	R/W	0x0	The output value of each GPIO. Used when the corresponding GPIO enable bits and GPIO output MUX registers are correctly set.

6.8.13 GPIO Output Enable Bits (H_GPIO_OE_BITS)

Address: 0x1000_404C
Access: Read/Write
Reset Value: 0000_0000

NOTE: Each 2-bit field controls the drive mechanism for each GPIO. The mapping for this 2-bit field is:

- 0 = Never drive output
- 1 = Drive if the output is low
- 2 = Drive if the output is high
- 3 = Always drive output

Bit	Bit Name	Type	Reset	Description	
31:30	GPIO_OE15	R/W	0x0	Configuration for GPIO15	
29:28	GPIO_OE14	R/W	0x0	Configuration for GPIO14	
27:26	GPIO_OE13	R/W	0x0	Configuration for GPIO13	
25:24	GPIO_OE12	R/W	0x0	Configuration for GPIO12	
23:22	GPIO_OE11	R/W	0x0	Configuration for GPIO11	
21:20	GPIO_OE10	R/W	0x0	Configuration for GPIO10	
19:18	GPIO_OE9	R/W	0x0	Configuration for GPIO9	
17:16	GPIO_OE8	R/W	0x0	Configuration for GPIO8	
15:14	GPIO_OE7	R/W	0x0	Configuration for GPIO7	
13:12	GPIO_OE6	R/W	0x0	Configuration for GPIO6	
11:10	GPIO_OE5	R/W	0x0	Configuration for GPIO5	
9:8	GPIO_OE4	R/W	0x0	Configuration for GPIO4	
7:6	GPIO_OE3	R/W	0x0	Configuration for GPIO3	
5:4	GPIO_OE2	R/W	0x0	Configuration for GPIO2	
3:2	GPIO_OE1	R/W	0x0	Configuration for GPIO1	
1:0	GPIO_OE0	R/W	0x0	Configuration for GPIO0	
				0	Never drive output
				1	Drive if the output is low
				2	Drive if the output is high
				3	Always drive output

6.8.14 GPIO Interrupt Polarity (H_GPIO_IRQ_POLAR)

Address: 0x1000_4050
Access: Read/Write
Reset Value: 0000_0000

Bit	Description	
31:16	Reserved	
15:0	GPIO interrupt polarity	
	0	Corresponding GPIO can interrupt the system if it is high
	1	Corresponding GPIO can interrupt system if it is low

6.8.15 GPIO Input Enable and Value (H_GP_INPT_EN_VAL)

Address: 0x1000_4054
Access: Read/Write
Reset Value: 0000_0000

Bit	Description	
31:18	Reserved	
17	0	JTAG enabled; GPIO[4:0] is controlled by JTAG controller
	1	JTAG disabled; software must set this bit before using GPIO[4:0]
16	0	RTC reset controlled entirely by software
	1	RTC reset controllable through a GPIO pin and software
15	0	Set RFSILENT_BB_L to default
	1	Connect RFSILENT_BB_L to a GPIO input
14:8	Reserved	
7	Default value of RFSILENT_BB_L input to the baseband	
6:0	Reserved	

6.8.16 GPIO Input MUX1 (H_GP_INPT_MUX1)

Address: 0x1000_4058
Access: Read/Write
Reset Value: 0000_0000

Bit	Description
31:8	Reserved
7:4	GPIO_INPUT_MUX[1] for GPIO_RST_AZM_TS_VAL input
3:0	GPIO_INPUT_MUX[0] for GPIO_RST_TSF_VAL input

6.8.17 GPIO Input MUX2 (H_GP_INPT_MUX2)

Address: 0x1000_405C
Access: Read/Write
Reset Value: 0000_E000

Bit	Description
31:12	Reserved
11:8	GPIO_INPUT_MUX[8] for RTC reset input
7:4	GPIO_INPUT_MUX[7] for RFSILENT_BB_1 input
3:0	Reserved

6.8.18 GPIO Output MUX1 (H_GP_OUTPT_MUX1)

Address: 0x1000_4060
Access: Read/Write
Reset Value: 0000_0000

NOTE: See Table 6-14.

Bit	Description
31:26	Reserved
29:25	GPIO_OUTPUT_MUX[5]
24:20	GPIO_OUTPUT_MUX[4]
19:15	GPIO_OUTPUT_MUX[3]
14:10	GPIO_OUTPUT_MUX[2]
9:5	GPIO_OUTPUT_MUX[1]
4:0	GPIO_OUTPUT_MUX[0]

6.8.19 GPIO Output MUX2 (H_GP_OUTPT_MUX2)

Address: 0x1000_4064
Access: Read/Write
Reset Value: 000E_8000

NOTE: See Table 6-14.

Bit	Description
31:30	Reserved
29:25	GPIO_OUTPUT_MUX[11]
24:20	GPIO_OUTPUT_MUX[10]
19:15	GPIO_OUTPUT_MUX[9]
14:10	GPIO_OUTPUT_MUX[8]
9:5	GPIO_OUTPUT_MUX[7]
4:0	GPIO_OUTPUT_MUX[6]

Table 6-14 shows the output MUX value for each GPIO.

Table 6-14. **Output MUX Values for Each GPIO**

Bit	Description
31	Set GPIO to BB_RADIO_XLNAON
30:29	Reserved
28	Set GPIO to RX_CLEAR_EXTENSION
27:8	Reserved
7	Reserved
6	Set GPIO to MAC power LED signal
5	Set GPIO to MAC network LED signal
4	Set GPIO to Rx-clear-external signal
3	Set GPIO to Tx-frame signal
2	Reserved
1	Reserved
0	Set GPIO output to value set in the GPIO output register

6.8.20 Input Values (H_INPUT_STATE)

Address: 0x1000_406C
Access: Read-Only
Reset Value: 0000_0013

Bit	Description
31:8	Reserved
7	Status of BB_RADIO_XLNAON from the BB
6	Status of TX_FRAME from the MAC
5	Status of RX_CLEAR_EXTERNAL from the MAC
4	Status of the power LED from the MAC
3	Status of the network LED from the MAC
2:0	Reserved

6.8.21 EEPROM Status and Read Data (H_EEP_STS_DATA)

Address: 0x1000_407C
Access: Read-Only
Reset Value: 0000_0000

Bit	Description	
31:20	Reserved	
19	This bit indicates that software attempted to access the EEPROM even though it is not present	
18	This bit indicates that the last software access to the EEPROM occurred to a protected area within the EEPROM and was therefore not forwarded to the EEPROM	
17	This bit indicates that the last software access to the EEPROM occurred when it was busy and was therefore not forwarded to the EEPROM	
16	0	EEPROM is idle
	1	EEPROM is busy
15:0	Results of the last EEPROM read transfer	

6.8.22 RFSilent-Related Registers (H_RFSILENT)

Address: 0x1000_4084
Access: Read/Write
Reset Value: 0000_0000

Bit	Description	
31:3	Reserved	
2	RTC reset invert This bit is only relevant if RTC reset override (bit [16]) in the "GPIO Input Enable and Value (H_GP_INPT_EN_VAL)" register is set. If the RTC reset override bit is cleared, then the RTC reset is entirely controlled by software (bit [0] of the register at 0x7040).	
	0	A low in the corresponding GPIO input holds the RTC in reset; a high allows the RTC reset to be controlled by software
	1	A high in the corresponding GPIO input holds the RTC in reset; a low allows the RTC Reset to be controlled by software
1	RFSILENT_FORCE signal to the baseband	
0	RFSilent polarity	
	0	Do not invert the RFSILENT_BB_L signal to the baseband
	1	Invert the RFSILENT_BB_L signal to the baseband

6.8.23 GPIO Pull-Up/Pull-Down (H_GPIO_PDPU)

Address: 0x1000_4088
Access: Read/Write
Reset Value: 0000_0001

NOTE: Each 2-bit field controls the drive mechanism for each GPIO. The mapping for this 2-bit field is:

- 0 = No pull-up or pull-down
- 1 = Pull-down
- 2 = Pull-up
- 3 = No pull-up or pull-down

Bit	Description
31:30	Configuration for GPIO15
29:28	Configuration for GPIO14
27:26	Configuration for GPIO13
25:24	Configuration for GPIO12
23:22	Configuration for GPIO11
21:20	Configuration for GPIO10
19:18	Configuration for GPIO9
17:16	Configuration for GPIO8
15:14	Configuration for GPIO7
13:12	Configuration for GPIO6
11:10	Configuration for GPIO5
9:8	Configuration for GPIO4
7:6	Configuration for GPIO3
5:4	Configuration for GPIO2
3:2	Configuration for GPIO1
1:0	Configuration for GPIO0

6.8.24 GPIO Drive Strength (H_GPIO_DS)

Address: 0x1000_408C
Access: Read/Write
Reset Value: 0000_0000

NOTE: Each 2-bit field corresponds to a particular value; the possibilities are:

- 0 = Default drive strength = 6 mA
- 1 = Drive strength = 12 mA
- 2 = Drive strength = 18 mA
- 3 = Drive strength = 24 mA

Bit	Description
31:30	Configuration for GPIO15
29:28	Configuration for GPIO14
27:26	Configuration for GPIO13
25:24	Configuration for GPIO12
22:23	Configuration for GPIO11
20:21	Configuration for GPIO10

Bit	Description
19:18	Configuration for GPIO9
17:16	Configuration for GPIO8
15:14	Configuration for GPIO7
13:12	Configuration for GPIO6
11:10	Configuration for GPIO5
9:8	Configuration for GPIO4
7:6	Configuration for GPIO3
5:4	Configuration for GPIO2
3:2	Configuration for GPIO1
1:0	Configuration for GPIO0

6.8.25 AHB Burst Mode (MAC_AHB_BURST_MODE)

Address: 0x1000_40B8
Access: Read/Write

This register is used to denote the burst mode for the AHB bus.

Bit	Bit Name	Type	Reset	Description
31:3	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
2	BURST_16_EN	R/W	0x0	Enables the 16-beat burst mode of the AHB bus
1	BURST_8_EN	R/W	0x0	Enables the 8-beat burst mode of the AHB bus
0	BURST_4_EN	R/W	0x0	Enables the 4-beat burst mode of the AHB bus

6.9 RTC Interface Registers

RTC registers occupy the address space 0x1000_7000 – 0x1000_7FFC in the memory of the ARXXXX. Within this address range, the 0x1000_7040 – 0x1000_7058 registers are always on and available for software access regardless of the sleep state of the RTC. Table 6-15 shows the mapping of these registers.

Table 6-15. **RTC Interface Registers (Always On)**

Address	Name	Description	Page
0x1000_7040	RTC_RESET	RTC Reset and Force Sleep and Force Wakeup	page 105
0x1000_7044	RTC_STATUS	RTC Sleep Status	page 105
0x1000_7048	RTC_DERIVED	RTC Force Derived RTC and Bypass Derived RTC	page 105
0x1000_704C	RTC_FORCE_WAKE	RTC Force Wake	page 105
0x1000_7050	RTC_INT_CAUSE	RTC Interrupt Cause	page 106
0x1000_7050	RTC_CAUSE_CLR	RTC Interrupt Cause Clear	page 106
0x1000_7054	RTC_INT_ENABLE	RTC Interrupt Enable	page 107
0x1000_7058	RTC_INT_MASK	RTC Interrupt Mask	page 107

6.9.1 RTC Reset and Force Sleep and Force Wakeup (RTC_RESET)

Address: 0x1000_7040
Access: Read/Write
Default: 0

Bit	Description
31:1	Reserved
0	RTC reset (active low)

6.9.2 RTC Sleep Status (RTC_STATUS)

Address: 0x1000_7044
Access: Read-Only
Default: N/A

Bit	Description
31:6	Reserved
5	PLL_CHANGING signal from RTC
4	RTC cold reset (active high)
3	RTC in wakeup state
2	RTC in sleep state
1	RTC in on state
0	RTC in shutdown state

6.9.3 RTC Force Derived RTC and Bypass Derived RTC (RTC_DERIVED)

Address: 0x1000_7048
Access: Read/Write
Default: 0

Bit	Description
31:2	Reserved
1	Force derived RTC
0	Bypass derived RTC

6.9.4 RTC Force Wake (RTC_FORCE_WAKE)

Address: 0x1000_704C
Access: Read/Write
Default: 3

Bit	Description	
31:2	Reserved	
1	0	Do not assert FORCE_WAKE on MAC interrupt
	1	Assert FORCE_WAKE on MAC interrupt
0	FORCE_WAKE signal to the MAC	

6.9.5 RTC Interrupt Cause (RTC_INT_CAUSE)

Address: 0x1000_7050
Access: Read-Only
Default: 0

NOTE: The RTC Interrupt controller works the same way as the host interface interrupt controller. Each bit in this interrupt cause register pertains to an event as described.

Bit	Description
31:6	Reserved
5	PLL_CHANGING
4	Software access of an RTC register when it is not in the on state
3	RTC in wakeup state
2	RTC in sleep state
1	RTC in on state
0	RTC in shutdown state

6.9.6 RTC Interrupt Cause Clear (RTC_CAUSE_CLR)

Address: 0x1000_7050
Access: Write-Only
Default: 0

NOTE: A write of 1 to any bit in this register clears that bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" register until the corresponding event reoccurs.

Bit	Description
31:6	Reserved
5	Writing 1 to this bit clears the PLL_CHANGING interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.
4	Writing 1 to this bit clears the software access of an RTC register interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.
3	Writing 1 to this bit clears the RTC in wakeup state interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.
2	Writing 1 to this bit clears the RTC in sleep state interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.
1	Writing 1 to this bit clears the RTC in on state interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.
0	Writing 1 to this bit clears the RTC in shutdown state interrupt from the "RTC Interrupt Cause (RTC_INT_CAUSE)" register.

6.9.7 RTC Interrupt Enable (RTC_INT_ENABLE)

Address: 0x1000_7054
Access: Read/Write
Default: 0

NOTE: Writing a 1 to any bit in this register allows that bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" register to be set when the corresponding event occurs. Writing a 0 to any bit in this register automatically clears the corresponding bit in the interrupt cause register regardless of the corresponding event.

Bit	Description	
31:6	Reserved	
5	0	Clears the PLL_CHANGING bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the PLL changing bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.
4	0	Clears the software access of an RTC register bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the software access of an RTC register bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.
3	0	Clears the RTC in wakeup state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the RTC in wakeup state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.
2	0	Clears the RTC in sleep state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the RTC in sleep state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.
1	0	Clears the RTC in on state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the RTC in on state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.
0	0	Clears the RTC in shutdown state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)".
	1	Allows the RTC in shutdown state bit in the "RTC Interrupt Cause (RTC_INT_CAUSE)" to be set when the corresponding event occurs.

6.9.8 RTC Interrupt Mask (RTC_INT_MASK)

Address: 0x1000_7058
Access: Read/Write
Default: 0

NOTE: Writing a 1 to any bit in this register allows the corresponding event to generate an RTC interrupt to the host interface which can in turn be programmed to generate a system interrupt. The corresponding bit in the "RTC Interrupt Enable (RTC_INT_ENABLE)" register must also be set.

Bit	Description
31:6	Reserved
5	Writing 1 to this bit allows the corresponding PLL_CHANGING event to generate an RTC interrupt to the host interface.
4	Writing 1 to this bit allows the corresponding software access of an RTC register event to generate an RTC interrupt to the host interface.
3	Writing 1 to this bit allows the corresponding RTC in wakeup state event to generate an RTC interrupt to the host interface.
2	Writing 1 to this bit allows the corresponding RTC in sleep state event to generate an RTC interrupt to the host interface.
1	Writing 1 to this bit allows the corresponding RTC in on state event to generate an RTC interrupt to the host interface.
0	Writing 1 to this bit allows the corresponding RTC in shutdown state event to generate an RTC interrupt to the host interface.

6.10 MAC Interface Registers

The MAC DMA occupies the address space 0x1000_0000 – 0x1000_1FFC. Within this 8 Kb range, the address range 0x1000_1F00 – 0x1000_1FFC consists of always-on registers available for software access regardless of the sleep state of the MAC.

Table 6-16 shows the mapping of these registers.

Table 6-16. **MAC Interface Registers**

Address	Access	Name	Description	Page
0x1000_1F00	R	MAC_SLEEP	MAC sleep status	page 108
0x1000_1F04	R/W	MAC_LED	MAC LED control	page 108

6.10.1 MAC Sleep Status (MAC_SLEEP)

Address: 0x1000_1F00
Access: Read-Only
Default Value: N/A

Bit	Description	
0	0	MAC is awake
	1	MAC is asleep

6.10.2 MAC LED Control (MAC_LED)

Address: 0x1000_1F04
Access: Read/Write
Default Value: 0

Bit	Description
11	Association pending
10	Association active
9:7	LED mode select
6:4	LED blink threshold select
3	LED slowest blink rate mode
2	LED hysteresis disable
1:0	Sleep clock rate

6.11 MAC PCU Registers

Table 6-17 shows the mapping of the MAC PCU registers and their allotted address space.

Table 6-17. **MAC PCU Registers**

Address	Name	Description	Page
0x1000_8000	MAC_PCU_STA_ADDR_L32	STA Address Lower 32 Bits	page 111
0x1000_8004	MAC_PCU_STA_ADDR_U16	STA Address Upper 16 Bits	page 111
0x1000_8008	MAC_PCU_BSSID_L32	BSSID Lower 32 Bits	page 112
0x1000_800C	MAC_PCU_BSSID_U16	BSSID Upper 16 Bits	page 112
0x1000_8010	MAC_PCU_BCN_RSSI_AVE	Beacon RSSI Average	page 112
0x1000_8014	MAC_PCU_ACK_CTS_TIMEOUT	ACK and CTS Timeout	page 113
0x1000_8018	MAC_PCU_BCN_RSSI_CTL	Beacon RSSI Control	page 113
0x1000_801C	MAC_PCU_USEC_LATENCY	Millisecond Counter and Rx/Tx Latency	page 113
0x1000_8020	MAC_PCU_RESET_TSF	Reset TSF	page 114
0x1000_8038	MAC_PCU_MAX_CFP_DUR	Maximum CFP Duration	page 114
0x1000_803C	MAC_PCU_RX_FILTER	Rx Filter	page 114
0x1000_8040	MAC_PCU_MCAST_FILTER_L32	Multicast Filter Mask Lower 32 Bits	page 115
0x1000_8044	MAC_PCU_MCAST_FILTER_U32	Multicast Filter Mask Upper 32 Bits	page 115
0x1000_8048	MAC_PCU_DIAG_SW	Diagnostic Switches	page 115
0x1000_804C	MAC_PCU_TSF_L32	TSF Lower 32 Bits	page 116
0x1000_8050	MAC_PCU_TSF_U32	TSF Upper 32 Bits	page 116
0x1000_8058	MAC_PCU_DEF_ANTENNA	Default Antenna	page 116
0x1000_805C	MAC_PCU_AES_MUTE_MASK_0	AES Mute Mask 0	page 117
0x1000_8060	MAC_PCU_AES_MUTE_MASK_1	AES Mute Mask 1	page 117
0x1000_8080	MAC_PCU_LAST_BEACON_TSF	Last Receive Beacon TSF	page 117
0x1000_8084	MAC_PCU_NAV	Current NAV	page 117
0x1000_8088	MAC_PCU_RTS_SUCCESS_CNT	Successful RTS Count	page 118
0x1000_808C	MAC_PCU_RTS_FAIL_CNT	Failed RTS Count	page 118
0x1000_8090	MAC_PCU_ACK_FAIL_CNT	FAIL ACK Count	page 118
0x1000_8094	MAC_PCU_FCS_FAIL_CNT	Failed FCS Count	page 118
0x1000_8098	MAC_PCU_BEACON_CNT	Beacon Count	page 119
0x1000_80B0	MAC_PCU_TX_ANT_1	MAC PCU Transmit Antenna 1	page 119
0x1000_80B4	MAC_PCU_TX_ANT_2	MAC PCU Transmit Antenna 2	page 119
0x1000_80B8	MAC_PCU_TX_ANT_3	MAC PCU Transmit Antenna 3	page 119
0x1000_80BC	MAC_PCU_TX_ANT_4	MAC PCU Transmit Antenna 4	page 119
0x1000_80D4	MAC_PCU_SLP1	Sleep 1	page 120
0x1000_80D8	MAC_PCU_SLP2	Sleep 2	page 120
0x1000_80E0	MAC_PCU_ADDR1_MASK_L32	Address 1 Mask Lower 32 Bits	page 120
0x1000_80E4	MAC_PCU_ADDR1_MASK_U16	Address 1 Mask Upper 16 Bits	page 120
0x1000_80E8	MAC_PCU_TPC	Tx Power Control	page 121
0x1000_80EC	MAC_PCU_TX_FRAME_CNT	Tx Frame Counter	page 121

Table 6-17. **MAC PCU Registers**

Address	Name	Description	Page
0x1000_80F0	MAC_PCU_RX_FRAME_CNT	Rx Frame Counter	page 121
0x1000_80F4	MAC_PCU_RX_CLEAR_CNT	Rx Clear Counter	page 121
0x1000_80F8	MAC_PCU_CYCLE_CNT	Cycle Counter	page 122
0x1000_80FC	MAC_PCU_QUIET_TIME_1	Quiet Time 1	page 122
0x1000_8100	MAC_PCU_QUIET_TIME_2	Quiet Time 2	page 122
0x1000_8108	MAC_PCU_QOS_NO_ACK	QoS no ACK	page 123
0x1000_810C	MAC_PCU_PHY_ERROR_MASK	PHY Error Mask	page 123
0x1000_8114	MAC_PCU_RXBUF_THRESHOLD	Rx Buffer Threshold	page 124
0x1000_8118	MAC_PCU_MIC_QOS_CONTROL	QoS Control	page 124
0x1000_811C	MAC_PCU_MIC_QOS_SELECT	Michael QoS Select	page 125
0x1000_8120	MAC_PCU_MISC_MODE	Miscellaneous Mode	page 125
0x1000_8124	MAC_PCU_FILTER_OFDM_CNT	Filtered OFDM Counter	page 126
0x1000_8128	MAC_PCU_FILTER_CCK_CNT	Filtered CCK Counter	page 126
0x1000_812C	MAC_PCU_PHY_ERR_CNT_1	PHY Error Counter 1	page 127
0x1000_8130	MAC_PCU_PHY_ERR_CNT_1_MASK	PHY Error Counter 1 Mask	page 127
0x1000_8134	MAC_PCU_PHY_ERR_CNT_2	PHY Error Counter 2	page 127
0x1000_8138	MAC_PCU_PHY_ERR_CNT_2_MASK	PHY Error Counter 2 Mask	page 128
0x1000_813C	MAC_PCU_TSF_THRESHOLD	TSF Threshold	page 128
0x1000_8144	MAC_PCU_PHY_ERROR_EIFS_MASK	PHY Error EIFS Mask	page 128
0x1000_8168	MAC_PCU_PHY_ERR_CNT_3	PHY Error Counter 3	page 128
0x1000_816C	MAC_PCU_PHY_ERR_CNT_3_MASK	PHY Error Counter 3 Mask	page 129
0x1000_8178	MAC_PCU_HCF_TIMEOUT	HCF Timeout	page 129
0x1000_81D0	MAC_PCU_TXSIFS	SIFS, Tx Latency and ACK Shift	page 129
0x1000_81EC	MAC_PCU_TXOP_X	TXOP for Non-QoS Frames	page 130
0x1000_81F0	MAC_PCU_TXOP_0_3	TXOP for TID 0 to 3	page 130
0x1000_81F4	MAC_PCU_TXOP_4_7	TXOP for TID 4 to 7	page 130
0x1000_81F8	MAC_PCU_TXOP_8_11	TXOP for TID 8 to 11	page 132
0x1000_81FC	MAC_PCU_TXOP_12_15	TXOP for TID 0 to 3	page 132
0x1000_8200	MAC_PCU_GENERIC_TIMERS[0:15]	Generic Timers	page 133
0x1000_8240	MAC_PCU_GENERIC_TIMERS_MODE	Generic Timers Mode	page 133
0x1000_8244	MAC_PCU_SLP32_MODE	32 KHz Sleep Mode	page 133
0x1000_8248	MAC_PCU_SLP32_WAKE	32 KHz Sleep Wake	page 134
0x1000_824C	MAC_PCU_SLP32_INC	32 KHz Sleep Increment	page 134
0x1000_8250	MAC_PCU_SLP_MIB1	Sleep MIB Sleep Count	page 134
0x1000_8254	MAC_PCU_SLP_MIB2	Sleep MIB Cycle Count	page 134
0x1000_8258	MAC_PCU_SLP_MIB3	Sleep MIB Control Status	page 135
0x1000_8284	US_SCALAR	Microsecond Scalar of the MAC Clock	page 135
0x1000_8318	MAC_PCU_20_40_MODE	Global Mode	page 135
0x1000_8328	MAC_PCU_RX_CLEAR_DIFF_CNT	Difference Rx_Clear Counter	page 135

Table 6-17. **MAC PCU Registers**

Address	Name	Description	Page
0x1000_8330	MAC_PCU_BA_BAR_CONTROL	Control Registers for Block BA Control Fields	page 136
0x1000_8334	MAC_PCU_LEGACY_PLCP_SPOOF	Legacy PLCP Spoof	page 136
0x1000_8338	MAC_PCU_PHY_ERROR_MASK_CONT	PHY Error Mask and EIFS Mask	page 136
0x1000_833C	MAC_PCU_TX_TIMER	Tx Timer	page 137
0x1000_8344	MAC_MISC_MODE2	MAC Miscellaneous Mode	page 137
0x1000_8800	MAC_PCU_KEY_CACHE[0:1023]	Key Cache Lower Half	page 138

6.11.1 STA Address Lower 32 Bits (MAC_PCU_STA_ADDR_L32)

Address: 0x1000_08000
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the STA address.

Bit	Name	Description
31:0	ADDR_31_0	Lower 32 bits of STA MAC address (PCU_STA_ADDR[31:0])

6.11.2 STA Address Upper 16 Bits (MAC_PCU_STA_ADDR_U16)

Address: 0x1000_08004
Access:Hardware = Read-Only
Software = Read/Write
Reset Value: 0x2000_0000

This register contains the lower 32 bits of the STA address.

Bit	Name	Description	
31	REG_ADHOC_MCAST_SEARCH	Enables the key cache search for ad hoc MCAST packets	
30	PCU_CBCIV_ENDIAN	Endianess of IV in CBC nonce	
29	REG_PRESERVE_SEQNUM	Stops PCU from replacing the sequence number; must be set to 1	
28	PCU_KSRCH_MODE	Search key cache first. If not, match use offset for IV = 0, 1, 2, 3. ■ If KSRCH_MODE = 0 then do not search ■ If IV = 1, 2, or 3, then search ■ If IV = 0, do not search	
27	REG_CRPT_MIC_ENABLE	Enables the checking and insertion of MIC in TKIP	
26	RES	Reserved	
25	PCU_BSRATE_11B	802.11b base rate	
		0	Use all rates
		1	Use only 1–2 Mbps
24	PCU_ACKCTS_6MB	Use 6 Mbps rate for ACK and CTS	
23	RTS_USE_DEF	RTS/CTS sent by the default antenna	

Bit	Name	Description
22	DEFANT_UPDATE	Enables swapping the default antenna upon odd retries
21	USE_DEFANT	Forces the antenna selection from the default antenna
20	PCU_PCF	Set if associated AP is PCF capable
19	PCU_NO_KEYSEARCH	Disable key search
18	PCU_PSMODE	Set if STA is in power-save mode
17	PCU_ADHOC	Set if STA is in an ad hoc network
16	PCU_AP	Set if STA is an AP
15:0	PCU_STA_ADDR[47:32]	Upper 16 bits of station MAC address

6.11.3 BSSID Lower 32 Bits (MAC_PCU_BSSID_L32)

Address: 0x1000_08008
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the BSS identification information.

Bit	Name	Description
31:0	PCU_BSSID[31:0]	Lower 32 bits of BSSID

6.11.4 BSSID Upper 16 Bits (MAC_PCU_BSSID_U16)

Address: 0x1000_0800C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

This register contains the upper 16 bits of the BSS identification information.

Bit	Name	Description
31:27	RES	Reserved
26:16	PCU_AID	Association ID
15:0	PCU_BSSID[47:32]	Upper 16 bits of BSSID

6.11.5 Beacon RSSI Average (MAC_PCU_BCN_RSSI_AVE)

Address: 0x1000_08010
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x800

Bit	Name	Description
31:12	RES	Reserved
11:0	REG_BCN_RSSI_AVE	Holds the average RSSI with 1/16 dB resolution. The RSSI is averaged over multiple beacons which matched our BSSID. AVE_VALUE is 12 bits with 4 bits below the normal 8 bits. These lowest 4 bits provide for a resolution of 1/16 dB. The averaging function depends on the BCN_RSSI_WEIGHT; determines the ratio of weight given to the current RSSI value compared to the average accumulated value.

6.11.6 ACK and CTS Timeout (MAC_PCU_ACK_CTS_TIMEOUT)

Address: 0x1000_08014
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29:16	PCU_CTS_TIMEOUT	Timeout while waiting for CTS (in cycles)
13:0	PCU_ACK_TIMEOUT	Timeout while waiting for ACK (in cycles)

6.11.7 Beacon RSSI Control (MAC_PCU_BCN_RSSI_CTL)

Address: 0x1000_08018
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:30	RES	Reserved
29	REG_BCN_RSSI_RST_STROBE	The BCN_RSSI_RESET clears "BCN_RSSI_AVE" to aid in changing channels
28:24	REG_BCN_RSSI_WEIGHT	Used to calculate "BCN_RSSI_AVE"
23:16	RES	Reserved
15:8	PCU_BCN_MISS_THR	Threshold at which the beacon miss interrupt asserts. Because the beacon miss counter increments at TBTT, it increments to 1 before the first beacon.
7:0	PCU_RSSI_THR	The threshold at which the beacon low RSSI interrupt is asserted when the average RSSI ("BCN_RSSI_AVE") below this level

6.11.8 Ms Counter and Rx/Tx Latency (MAC_PCU_USEC_LATENCY)

Address: 0x1000_0801C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:29	RES	Reserved
28:23	PCU_RXDELAY	Baseband Rx latency to start of SIGNAL (in µs)
22:14	PCU_TXDELAY	Baseband Tx latency to start of timestamp in beacon frame (in µs)
13:0	RES	Reserved

6.11.9 Reset TSF (MAC_PCU_RESET_TSF)

Address: 0x1000_08020
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Controls beacon operation by the PCU.

Bit	Name	Description
31:25	RES	Reserved
24	ONE_SHOT	Setting this bit causes the TSF to reset. This register clears immediately after being reset.
23:0	RES	Reserved

6.11.10 Maximum CFP Duration (MAC_PCU_MAX_CFP_DUR)

Address: 0x1000_08038
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Contains the maximum time for a CFP.

Bit	Name	Description
31:16	RES	Reserved
15:0	PCU_MAX_CFPDUR	Maximum contention free period duration (in µs)

6.11.11 Rx Filter (MAC_PCU_RX_FILTER)

Address: 0x1000_0803C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register determines Rx frame filtering.

NOTE: If any bit is set, the corresponding packet types pass the filter and are DMAed. All filter conditions except the promiscuous setting rely on the no early PHY error and protocol version being checked to ensure it is version 0.

Bit	Name	Description	
31:10	RES	Reserved	
15	MCAST_BCAST_ALL	Enables receipt of all multicast and broadcast frames	
14	PS_POLL	Enables receipt of PS-POLL	
13:10	RES	Reserved	
9	MY_BEACON	Retrieves any beacon frame with matching SSID	
8	RES	Reserved	
7	PROBE_REQ	Probe request enable. Enables reception of all probe request frames	
6	RES	Reserved	
5	PROMISCUOUS	Promiscuous receive enable; Enable reception of all frames, including errors	
4	BEACON	Beacon frame enable; Enable reception of beacon frames.	
3	CONTROL	Control frame enable; Enable reception of control frames	
2	BROADCAST	Broadcast frame enable Enable reception of non beacon broadcast frames that originate from the BSS whose ID matches BSSID	
1	MULTICAST	Multicast frame enable Enable reception of multicast frames that match the multicast filter	
0	UNICAST	Unicast frame Enable Enable reception of unicast (directed) frames that match the STA address	
		0	Disable. No ACK will return
		1	Enable

6.11.12 Multicast Filter Mask Lower 32 Bits (MAC_PCU_MCAST_FILTER_L32)

Address: 0x1000_08040
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the lower 32 bits of the multicast filter mask.

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask low. Lower 32 bits of multicast filter mask.

6.11.13 Multicast Filter Mask Upper 32 Bits (MAC_PCU_MCAST_FILTER_U32)

Address: 0x1000_08044
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

This register contains the upper 32 bits of the multicast filter mask.

Bit	Name	Description
31:0	PCU_MCAST_MASK	Multicast filter mask high. Upper 32 bits of multicast filter mask.

6.11.14 Diagnostic Switches (MAC_PCU_DIAG_SW)

Address: 0x1000_08048
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Controls the operation of the PCU, including enabling/disabling acknowledgements, CTS, transmission, reception, encryption, loopback, FCS, channel information, and scrambler seeds.

Bit	Name	Description
31:30	RES	Reserved
29	RX_CLEAR_EXT_LOW	Force the RX_CLEAR_EXT signal to appear to the MAC as being low
28	RX_CLEAR_CTL_LOW	Force the RX_CLEAR_CTL signal to appear to the MAC as being low
27	RES	Reserved
26	SATURATE_CYCLE_CNT	The saturate cycle count bit, if set, causes the "Cycle Counter (MAC_PCU_CYCLE_CNT)" register to saturate instead of shifting to the right by 1 every time the count reaches 0xFFFFFFFF. This saturate condition also holds the rx_clear, rx_frame, and tx_frame counts.
25	FORCE_RX_ABORT	Force Rx abort bit in conjunction with Rx block aids quick channel change to shut down Rx. The force Rx abort bit kills with the Rx_abort any frame currently transferring between the MAC and baseband while the RX block bit prevents any new frames from getting started.
24:23	RES	Reserved
22	CHAN_IDLE_HIGH	Force channel idle high
21	IGNORE_NAV	Ignore virtual carrier sense (NAV)
20	RX_CLEAR_HIGH	Force RX_CLEAR high
19:18	RES	Reserved
17	ACCEPT_NON_V0	Enable or disable protocol field
16:8	RES	Reserved
7	CORRUPT_FCS	Enable or disable corrupt FCS. Enabling this bit causes an invalid FCS to be appended to a frame during transmission.
6	LOOP_BACK	Enable or disable Tx data loopback
5	HALT_RX	Enable or disable reception

Bit	Name	Description
4	NO_DECRYPT	Enable or disable decryption
3	NO_ENCRYPT	Enable or disable encryption
2	NO_CTS	Enable or disable CTS generation
1	NO_ACK	Enable or disable acknowledgement generation for all frames
0	PCU_INVALKEY_NOACK	Enable or disable acknowledgement when a valid key is not found for the received frames in the key cache.

6.11.15 TSF Lower 32 Bits (MAC_PCU_TSF_L32)

Address: 0x1000_0804C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs. Writes to this register do not cause the TSF to change. Rather, the value is held in a temporary staging area until this register is written, at which point both the lower and upper parts of the TSF are loaded. A read result of 0xFFFFFFFF indicates that the read occurred before TSF logic came out of sleep. It may take up to 45 µs after the chip is brought out of sleep for the TSF logic to wake.

6.11.16 TSF Upper 32 Bits (MAC_PCU_TSF_U32)

Address: 0x1000_08050
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0xFFFFFFF

Bit	Name	Description
31:0	VALUE	The timestamp value in µs

6.11.17 Default Antenna (MAC_PCU_DEF_ANTENNA)

Address: 0x08058
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description	
31:30	RES	Reserved	
29	FAST_TX_ANT_EN	Enables the fast Tx antenna diversity	
28	RX_LNA_CONFIG_SEL	The selection of the LNA configuration for Rx antenna diversity	
		0	Baseband uses the main LNA configuration
		1	Baseband uses the alternate LNA configuration
27	FAST_DEF_ANT	Default antenna setting for the fast Tx antenna diversity	
		0	Baseband uses antenna 1
		1	Baseband uses antenna 2
26	TX_CUR_ANT	Indicates the current antenna setting for fast Tx antenna diversity. SW can set this bit like the FAST_DEF_ANT upon startup.	

Bit	Name	Description	
25	SLOW_TX_ANT_EN	Enables the slow Tx antenna diversity. If this bit is set to 1, it will use the antenna which is carried in the Tx descriptor.	
24	TX_DEF_ANT_SEL	The default antenna setting for Tx antenna diversity	
		0	Baseband uses antenna 1
		1	Baseband uses antenna 2
23:0	RES	Reserved	

6.11.18 AES Mute Mask 0 (MAC_PCU_AES_MUTE_MASK_0)

Address: 0x1000_0805C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFF_C7FF

Bit	Name	Description
31:16	QOS_MUTEMASK	AES mute mask for TID field
15:0	FC_MUTEMASK	AES mute mask for frame control field

6.11.19 AES Mute Mask 1(MAC_PCU_AES_MUTE_MASK_1)

Address: 0x1000_08060
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xE7FF_000F

Bit	Name	Description
31:16	FC_MGMT	AES mute mask for management frame control field
15:0	SEQ_MUTEMASK	AES mute mask for sequence number field

6.11.20 Last Rx Beacon TSF (MAC_PCU_LAST_BEACON_TSF)

Address: 0x1000_08080
Access: Hardware = Write-only
Software = Read-Only
Reset Value: 0x0

Bit	Name	Description
31:0	LAST_TSTP	Beacon timestamp. Lower 32 bits of timestamp of the last beacon received.

6.11.21 Current NAV (MAC_PCU_NAV)

Address: 0x1000_08084
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:26	RES	Reserved
25:0	CS_NAV	Current NAV value (in µs)

6.11.22 Successful RTS Count (MAC_PCU_RTS_SUCCESS_CNT)

Address: 0x1000_08088
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of successful RTS exchanges. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_OK	RTS/CTS exchange success counter

6.11.23 Failed RTS Count (MAC_PCU_RTS_FAIL_CNT)

Address: 0x1000_0808C
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed RTS exchanges. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	RTS_FAIL	RTS/CTS exchange failure counter

6.11.24 FAIL ACK Count (MAC_PCU_ACK_FAIL_CNT)

Address: 0x1000_08090
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed acknowledgements. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	ACK_FAIL	DATA/ACK failure counter

6.11.25 Failed FCS Count (MAC_PCU_FCS_FAIL_CNT)

Address: 0x1000_08094
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of failed frame check sequences. The counter stops at 0xFFFF. After a read, this register is automatically reset to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	FCS_FAIL	FCS failure counter

6.11.26 Beacon Count (MAC_PCU_BEACON_CNT)

Address: 0x1000_08098
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

This register counts the number of valid beacon frames received. The counter stops at 0xFFFF. After a read, automatically resets to 0.

Bit	Name	Description
31:16	RES	Reserved
15:0	BEACONCNT	Valid beacon counter

6.11.27 Max PCU Transmit Antenna 1(MAC_PCU_TX_ANT_1)

Address: 0x1000_080B0
Access: Read/Write

This register is used to set the key cache antenna setting for Tx antenna diversity.

Bit	Bit Name	Type	Reset	Description
31:0	VALUE	R/W	0x0	The key cache antenna setting for fast Tx antenna diversity for client 0-31

6.11.28 Max PCU Transmit Antenna 2 (MAC_PCU_TX_ANT_2)

Address: 0x1000_080B4
Access: Read/Write

This register is used to set the key cache antenna setting for Tx antenna diversity.

Bit	Bit Name	Type	Reset	Description
31:0	VALUE	R/W	0x0	The key cache antenna setting for fast Tx antenna diversity for client 32-63

6.11.29 Max PCU Transmit Antenna 3 (MAC_PCU_TX_ANT_3)

Address: 0x1000_080B8
Access: Read/Write

This register is used to set the key cache antenna setting for Tx antenna diversity.

Bit	Bit Name	Type	Reset	Description
31:0	VALUE	R/W	0x0	The key cache antenna setting for fast Tx antenna diversity for client 64-95

6.11.30 Max PCU Transmit Antenna 4 (MAC_PCU_TX_ANT_4)

Address: 0x1000_080BC
Access: Read/Write

This register is used to set the key cache antenna setting for Tx antenna diversity.

Bit	Bit Name	Type	Reset	Description
31:0	VALUE	R/W	0x0	The key cache antenna setting for fast Tx antenna diversity for client 96-127

6.11.31 Sleep 1 (MAC_PCU_SLP1)

Offset: 0x1000_080D4
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

The Sleep 1 register in conjunction with the "Sleep 2 (MAC_PCU_SLP2)" register, controls when the AR9271 should wake when waiting for AP Rx traffic. Sleep registers are only used when the AR9271 is in STA mode.

Bit	Name	Description
31:21	CAB_TIMEOUT	Time in TU that the PCU waits for CAB after receiving the beacon or the previous CAB, insuring that if no CAB is received after the beacon is received or if a long gap occurs between CABs, the CAB powersave state returns to idle.
20	RES	Reserved
19	ASSUME_DTIM	A mode bit which indicates whether to assume a beacon was missed when the SLP_BEACON_TIMEOUT occurs with no received beacons, in which case is assumes the DTIM was missed, and waits for CAB.
18:0	RES	Reserved

6.11.32 Sleep 2 (MAC_PCU_SLP2)

Offset: 0x1000_080D8
Access: Hardware = Read/Write
Software = Read-Only
Reset Value: 0x0

Bit	Name	Description
31:21	BEACON_TIMEOUT	Time in TU that the PCU waits for a beacon after waking up. If this time expires, the PCU woke due to SLP_NEXT_DTIM, and SLP_ASSUME_DTIM is active, then it assumes the beacon was missed and goes directly to watching for CAB. Otherwise when this time expires, the beacon powersave state returns to idle.
20:0	RES	Reserved

6.11.33 Address 1 Mask Lower 32 Bits (MAC_PCU_ADDR1_MASK_L32)

Offset: 0x1000_080E0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFFFFFF

This STA register provides multiple BSSID support when the AR9271 is in AP mode.

Bit	Name	Description
31:0	STA_MASK_L	STA address mask lower 32-bit register. Provides multiple BSSID support.

6.11.34 Address 1 Mask Upper 16 Bits (MAC_PCU_ADDR1_MASK_U16)

Offset: 0x1000_080E4
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xFFFF

This STA register provides multiple BSSID support when the AR9271 is in AP mode.

Bit	Name	Description
31:0	STA_MASK_L	STA address mask upper 16-bit register. Provides multiple BSSID support.

6.11.35 Tx Power Control (MAC_PCU_TPC)

Offset: 0x1000_080E8
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x003F_3F3F

This register set the transmit power for self-generated response frames.

Bit	Name	Description
31:22	RES	Reserved
21:16	CHIRP_PWR	Chirp self-generated response frames
15:14	RES	Reserved
13:8	CTS_PWR	CTS self-generated response frames
7:6	RES	Reserved
5:0	ACK_PWR	ACK self-generated response frames

6.11.36 Tx Frame Counter (MAC_PCU_TX_FRAME_CNT)

Offset: 0x1000_080EC
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The Tx frame counter counts the number of cycles the tx_frame signal is active.

Bit	Name	Description
31:0	TX_FRAME_CNT	Counts the number of cycles the tx_frame signal is active

6.11.37 Rx Frame Counter (MAC_PCU_RX_FRAME_CNT)

Offset: 0x1000_080F0
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The receive frame counter counts the number of cycles the rx_frame signal is active.

Bit	Name	Description
31:0	RX_FRAME_CNT	Counts the number of cycles the rx_frame signal is active

6.11.38 Rx Clear Counter (MmAC_PCU_RX_CLEAR_CNT)

Offset: 0x1000_080F4
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The receive clear counter counts the number of cycles the rx_clear signal is not active.

Bit	Name	Description
31:0	RX_CLEAR_CNT	Counts the number of cycles the rx_clear signal is low

6.11.39 Cycle Counter (MAC_PCU_CYCLE_CNT)

Offset: 0x1000_080F8
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The cycle counter counts the number of clock cycles.

Bit	Name	Description
31:0	CYCLE_CNT	Counts the number of clock cycles

6.11.40 Quiet Time 1 (MAC_PCU_QUIET_TIME_1)

Offset: 0x1000_080FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

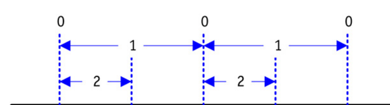
Bit	Name	Description
31:18	RES	Reserved
17	QUIET_ACK_CTS_ENABLE	If set, then the MAC sends an ACK or CTS in response to a received frame
16:0	RES	Reserved

6.11.41 Quiet Time 2 (MAC_PCU_QUIET_TIME_2)

Offset: 0x1000_080FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

The Quiet Time registers implement the quiet time function specified in the proposed 802.11h extension supporting radar detection.

NOTE: QUIET_ENABLE is implemented as GENERIC_TIMER_ENABLE and NEXT_QUIET as GENERIC_TIMER_NEXT. QUIET_PERIOD is implemented as GENERIC_TIMER_PERIOD.



- 0 = NEXT_QUIET = TSF[31:0]
- 1 = QUIET_PERIOD
- 2 = QUIET_DURATION
  (Chip remains awake during QUIET_DURATION)

Bit	Name	Description
31:16	QUIET_DURATION	The length of time in TUs that the chip is required to be quiet
15:0	RES	Reserved

6.11.42 QoS No ACK (MAC_PCU_QOS_NO_ACK)

Offset: 0x1000_08108
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x52

This register provides a mechanism to locate the NoACK information in the QoS field and determine which encoding means NOACK.

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Description</th></tr>
<tr><td>31:9</td><td>RES</td><td colspan="2">Reserved</td></tr>
<tr><td>8:7</td><td>NOACK_BYTE_OFFSET</td><td colspan="2">Number of bytes from the byte after end of the header of a data packet to the byte location where No Ack information is stored. (The end of the header is at byte offset 25 for 3-address packets and 31 for 4-address packets.)</td></tr>
<tr><td>6:4</td><td>NOACK_BIT_OFFSET</td><td colspan="2">Offsets from the byte where the No Ack information should be stored; offset can range from 0 to 6 only</td></tr>
<tr><td rowspan="6">3:0</td><td rowspan="6">NOACK_2_BIT_VALUES</td><td colspan="2">These values are of a two bit field that indicate No ACK</td></tr>
<tr><th>NOACK_2_BIT_VALUE</th><th>Encoding Matching No ACK</th></tr>
<tr><td>xxx1</td><td>00</td></tr>
<tr><td>xx1x</td><td>01</td></tr>
<tr><td>x1xx</td><td>10</td></tr>
<tr><td>1xxx</td><td>11</td></tr>
</table>

6.11.43 PHY Error Mask (MAC_PCU_PHY_ERROR_MASK)

Offset: 0x1000_0810C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x2

NOTE: Provides the ability to choose which PHY errors from the baseband to filter. The error number offsets into this register. If the mask value at the offset is 0, this error filters and does not show up on the Rx queue.

Bit	Name	Description
31	ERROR CCK RESTART	CCK restart error
30	ERROR CCK SERVICE	CCK service error
29:28	RES	Reserved
27	ERROR CCK RATE_ILLEGAL	CCK illegal rate error
26	ERROR CCK HEADER_CRC	CCK CRC header error
25	ERROR CCK TIMING	False detection for CCK
24	RES	Reserved
23	ERROR OFDM RESTART	OFDM restart error
22	ERROR OFDM SERVICE	OFDM service error
21	ERROR OFDM POWER_DROP	OFDM power drop error
20	ERROR OFDM LENGTH_ILLEGAL	OFDM illegal length error
19	ERROR OFDM RATE_ILLEGAL	OFDM illegal rate error
18	ERROR OFDM SIGNAL_PARITY	OFDM signal parity error
17	ERROR OFDM TIMING	False detection for OFDM
16:8	RES	Reserved

Bit	Name	Description
7	ERROR TX_INTERRUPT_RX	Transmit interrupt
6	ERROR ABORT	Abort error
5	ERROR RADAR_DETECT	Radar detect error
4	ERROR PANIC	Panic error
3:1	RES	Reserved
0	ERROR TRANSMIT_UNDERRUN	Transmit underrun error

6.11.44 Rx Buffer Threshold (MAC_PCU_RXBUF_THRESHOLD)

Offset: 0x1000_08114
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x400

Bit	Name	Description
31:11	RES	Reserved
10:0	RXBUF_THRSHD	When the number of valid entries in the Rx buffer is larger than this threshold, host interface logic gives higher priority to the Rx side to prevent Rx buffer overflow.

6.11.45 QoS Control (MAC_PCU_MIC_QOS_CONTROL)

Offset: 0x1000_08118
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0xAA

Bit	Name	Description	
31:17	RES	Reserved	
16	MIC_QOS_ENABLE	Enable MIC QOS control	
		0	Disable hardware Michael
		1	Enable hardware Michael
15:14	MIC_QOS_CONTROL [7]	MIC QOS control [7]. See options for "MIC_QOS_CONTROL [0]".	
13:12	MIC_QOS_CONTROL [6]	MIC QOS control [6]. See options for "MIC_QOS_CONTROL [0]".	
11:10	MIC_QOS_CONTROL [5]	MIC QOS control [5]. See options for "MIC_QOS_CONTROL [0]".	
9:8	MIC_QOS_CONTROL [4]	MIC QOS control [4]. See options for "MIC_QOS_CONTROL [0]".	
7:6	MIC_QOS_CONTROL [3]	MIC QOS control [3]. See options for "MIC_QOS_CONTROL [0]".	
5:4	MIC_QOS_CONTROL [2]	MIC QOS control [2]. See options for "MIC_QOS_CONTROL [0]".	
3:2	MIC_QOS_CONTROL [1]	MIC QOS control [1]. See options for "MIC_QOS_CONTROL [0]".	
1:0	MIC_QOS_CONTROL [0]	MIC QOS control [0]	
		0	Use 0 when calculating Michael
		1	Use 1 when calculating Michael
		2	Use MIC_QOS_SELECT when calculating Michael
		3	Use inverse of MIC_QOS_SELECT when calculating Michael

6.11.46 Michael QoS Select (MAC_PCU_MIC_QOS_SELECT)

Offset: 0x1000_0811C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x3210

Bit	Name	Description
31:28	MIC_QOS_SELECT [7]	MIC QOS select [7]. Select the OOS TID bit when calculating Michael.
27:24	MIC_QOS_SELECT [6]	MIC QOS select [6]. Select the OOS TID bit when calculating Michael.
23:20	MIC_QOS_SELECT [5]	MIC QOS select [5]. Select the OOS TID bit when calculating Michael.
19:16	MIC_QOS_SELECT [4]	MIC QOS select [4]. Select the OOS TID bit when calculating Michael.
15:12	MIC_QOS_SELECT [3]	MIC QOS select [3]. Select the OOS TID bit when calculating Michael.
11:8	MIC_QOS_SELECT [2]	MIC QOS select [2]. Select the OOS TID bit when calculating Michael.
7:4	MIC_QOS_SELECT [1]	MIC QOS select [1]. Select the OOS TID bit when calculating Michael.
3:0	MIC_QOS_SELECT [0]	MIC QOS select [0]. Select the OOS TID bit when calculating Michael.

6.11.47 Miscellaneous Mode (MAC_PCU_MISC_MODE)

Offset: 0x1000_08120
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x8F24800

Bit	Name	Description
31:29	RES	Reserved
28	ALWAYS_PERFORM _ KEY_SEARCH	If this bit is set, key search is performed for every frame in an aggregate. If this bit is cleared, key search is only performed for the first frame of an aggregate. Unless the transmitter address is different between the frames in an aggregate. This bit has no effect on non-aggregate frame packets.
27	SEL_EVM	If the SEL_EVM bit is set, the evm field of the Rx descriptor status contains the EVM data received from the baseband. If this bit is cleared, the evm field of the Rx descriptor status contains 3 bytes of Legacy PLCP, 2 service bytes, and 6 bytes of HP PLCP.
26	CLEAR_BA_VALID	If the CLEAR_BA_VALID bit is set, the state of the block ACK storage is invalidated.
25	CLEAR_FIRST_HCF	If the CLEAR_FIRST_HCF bit is set, then the first_hcf state will be cleared. Set this bit to enter fast channel change mode and clear the bit once fast channel change is over.
24	CLEAR_VMF	If the CLEAR_VMF bit is set, then the VMF mode in the transmit state machine will be cleared. Set this bit to enter fast channel change mode and clear it once fast channel change is over.
23	RX_HCF_POLL _ENABLE	If the RX_HCF_POLL_ENABLE bit is set, then the MAC is enabled to receive directed HCF polls. If this bit is not set the receive state machine does not tell the rest of the MAC that it has received a directed HCF poll.
22	HCF_POLL _CANCELS_NAV	If the HCF_POLL_CANCELS_NAV bit is set when a directed HCF poll is received, the current NAV is cancelled and HCF data burst can proceed at SIFS.
21	TBTT_PROTECT	If the TBTT_PROTECT bit is set, then the time from TBTT to 20 µs after TBTT is protected from transmit. Turn this off in ad hoc mode or if this MAC is used in the AP.

Bit	Name	Description
20:19	RES	Reserved
18	FORCE_QUIET_ COLLISION	If the FORCE_QUIET_COLLISION bit is set, the PCU thinks that it is in quiet collision period, kills any transmit frame in progress, and prevents any new frame from starting.
17:13	RES	Reserved
12	TXOP_TBTT_LIMIT_ ENABLE	If this limit is set, then logic to limit the value of the duration to fit the time remaining in TXOP and time remaining until TBTT is turned on. This logic will also filter frames, which will exceed TXOP.
11:5	RES	Reserved
4	CCK_SIFS_MODE	If the CCK_SIFS_MODE is set, the chip assumes that it is using 802.11g mode where SIFS is set to 10 µs and non-CCK frames must add 6 to SIFS to make it CCK frames. This bit is needed in the duration calculation, which also needs the SIFS_TIME register.
3	TX_ADD_TSF	If the TX_ADD_TSF bit is set, the TSF in the transmit packet will be added to the internal TSF value for transmit beacons and probe_response frames.
2	MIC_NEW_ LOCATION_ ENABLE	If MIC_NEW_LOCATION_ENABLE is set, the Tx Michael Key is assumed to be co-located in the same entry that the Rx Michael key is located.
1	RES	Reserved
0	BSSID_MATCH_FOR CE	If the BSSID_MATCH_FORCE bit is set, all logic based on matching the BSSID thinks that the BSSID matches.

6.11.48 Filtered OFDM Counter (MAC_PCU_FILTER_OFDM_CNT)

Offset: 0x1000_08124
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

The filtered OFDM counters use the MIB control signals.

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTOFDM_CNT	Counts the OFDM frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

6.11.49 Filtered CCK Counter (MAC_PCU_Filter_CCK_CNT)

Offset: 0x1000_08128
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	FILTCCK_CNT	Counts the CCK frames that were filtered using MIB control signals. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

6.11.50 PHY Error Counter 1 (MAC_PCU_PHY_ERR_CNT_1)

The PHY error counters count any PHY error matching the respective mask. The bits of the 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FC, then all PHY errors from 2-7 and 24-31 are counted.

Address: 0x1000_0812C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT_1	The count of PHY errors that pass the PHY_ERR_CNT_1_MASK filter. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

6.11.51 PHY Error Counter 1 Mask (MAC_PCU_PHY_ERR_CNT_1_MASK)

Address: 0x1000_08130
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK1	Mask of the PHY error number allowed to be counted in the PHY error counter 1 register. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

6.11.52 PHY Error Counter 2 (MAC_PCU_PHY_ERR_CNT_2)

The PHY error counters count any PHY error matching the respective mask. The bits of the 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FC, then all PHY errors from 2-7 and 24-31 are counted.

Address: 0x1000_08134
Access: Hardware = Read/Write

Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
23:0	PHY_ERROR_CNT_2	The count of PHY errors that pass the PHY_ERR_CNT_2_MASK filter The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.
31:24	RES	Reserved

6.11.53 PHY Error Counter 2 Mask (MAC_PCU_PHY_ERR_CNT_2_MASK)

Address: 0x1000_08138
Reset Value: 0x0
Access: Hardware = Read-Only
Software = Read/Write

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK2	Mask of the PHY error number allowed to be counted in the PHY error counter 2 register. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

6.11.54 TSF Threshold (MAC_PCU_TSF_THRESHOLD)

Address: 0x1000_0813C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:16	RES	Reserved
15:0	TSF_THRESHOLD	Asserts the PCU_TSF_OUT_OF_RANGE_INTER if the corrected receive TSF in a beacon is different from the internal TSF by more than this threshold.

6.11.55 PHY Error EIFS Mask (MAC_PCU_PHY_ERROR_EIFS_MASK)

Address: 0x1000_08144
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	VALUE	This mask provides the ability to choose which PHY errors from the baseband cause EIFS delay. The error number is used as an offset into this mask. If the mask value at the offset is 1, then this error will not cause EIFS delay.

6.11.56 PHY Error Counter 3 (MAC_PCU_PHY_ERR_CNT_3)

The PHY error counters count any PHY error matching the respective mask. The bits of the 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to provide flexibility in counting. For example, if setting the mask bits to 0xFF0000FC, then all PHY errors from 2-7 and 24-31 are counted.

Address: 0x1000_08168

Access: Hardware = Read/Write
Software = Read/Write

Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:0	PHY_ERROR_CNT_3	The count of PHY errors that pass the PHY_ERR_CNT_3_MASK filter. The MIB freeze register holds all the values of these registers, and MIB zeros out all the values of these registers. MIB forces incrementation of all registers in each cycle. This counter saturates at the highest value and is writable. If the upper two bits of these counters are b11, PCU_MIB_THRESHOLD is asserted and an interrupt generated.

6.11.57 PHY Error Counter 3 Mask (MAC_PCU_PHY_ERR_CNT_3_MASK)

Address: 0x1000_0816C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	PHY_ERROR_CNT_MASK3	Mask of the PHY error number allowed to be counted in the PHY error counter 3 register. The values of any 32-bit masks correspond to the first 32 encoded values of the error. Setting multiple bits in the mask provides an ORing function to allow counting flexibility (e.g., setting the mask to 0xFF0000FF means all PHY errors from 0:7 and 24:31 are counted).

6.11.58 HCF Timeout (MAC_PCU_HCF_TIMEOUT)

Address: 0x1000_08178
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:16	RES	Reserved
15:0	VALUE	The time the PCU waits after the HCF trigger timer occurs before the PCU returns to sleep mode, unless the HCF poll has been detected. An interrupt is generated if the timeout occurs before a HCF poll is detected.

6.11.59 SIFS, Tx Latency and ACK Shift (MAC_PCU_TXSIFS)

Address: 0x1000_081D0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:15	RES	Reserved

Bit	Name	Description	
14:12	ACK_SHIFT	ACK_SHIFT is used to generate the ACK_TIME, which is used to generate the ACK_SIFS_TIME. The ACK_TIME table in the hardware assumes a channel width of 2.5 MHz. This value should be 3 for CCK rates.	
		0	2.5 MHz
		1	5 MHz
		2	10 MHz
		3	20 MHz (Standard 802.11g)
		4	40 MHz
11:8	TX_LATENCY	TX_LATENCY is the latency in µs from tx_frame being asserted by the MAC to when the energy of the frame is on the air. This value is used to decrease the time to TBTT and time remaining in TXOP in the calculation to determine quiet collision.	
7:0	SIFS_TIME	SIFS_TIME is the number of µs in SIFS	

6.11.60 TxOP for Non-QoS Frames (MAC_PCU_TXOP_X)

Address: 0x1000_081EC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:8	RES	Reserved
7:0	SIFS_TIME	TXOP in units of 32 µs. A TXOP value exists for each QOS TID value. When a new burst starts, the TID is used to select one of the 16 TXOP values. This TXOP decrements until the end of the burst to make sure that the packets are not sent out by the time TXOP expires. TXOPX is used for legacy non QOS bursting.

6.11.61 TxOP for TID 0 to 3 (MAC_PCU_TXOP_0_3)

Address: 0x1000_081F0
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_3	Value in units of 32 µs
23:16	VALUE_2	Value in units of 32 µs
15:8	VALUE_1	Value in units of 32 µs
7:0	VALUE_0	Value in units of 32 µs

6.11.62 TXOP for TID 4 to 7 (MAC_PCU_TXOP_4_7)

Address: 0x1000_081F4
Reset Value: 0x0
Access: Hardware = Read-Only
Software = Read/Write

Bit	Name	Description
31:24	VALUE_7	Value in units of 32 µs
23:16	VALUE_6	Value in units of 32 µs
15:8	VALUE_5	Value in units of 32 µs
7:0	VALUE_4	Value in units of 32 µs

6.11.63 TXOP for TID 8 to 11 (MAC_PCU_TXOP_8_11)

Address: 0x1000_081F8
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_11	Value in units of 32 µs
23:16	VALUE_10	Value in units of 32 µs
15:8	VALUE_9	Value in units of 32 µs
7:0	VALUE_8	Value in units of 32 µs

6.11.64 TXOP for TID 0 to 3 (MAC_PCU_TXOP_12_15)

Address: 0x1000_081FC
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	VALUE_15	Value in units of 32 µs
23:16	VALUE_14	Value in units of 32 µs
15:8	VALUE_13	Value in units of 32 µs
7:0	VALUE_12	Value in units of 32 µs

Generic Timers (MAC_PCU_GENERIC_TIMERS[0:15])

Offset: 0x08200
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Address	Default	Description
0x8200–0x821C	0x0	GENERIC_TIMER_NEXT
0x8220–0x823C	0x0	GENERIC_TIMER_PERIOD

NOTE: GENERIC _TIMER_0, unlike other generic timers, does not wake the MAC before timer expiration and its overflow mechanism does not generate an interrupt. Instead, it silently adds this period repeatedly until the next timer advances past the TSF. Thus when MAC wakes after sleeping for multiple TBTTs, the TGBTT does not assert repeatedly or cause the beacon miss count to jump.

Generic Timer	Function
0	TBTT
1	DMA beacon alert
2	SW beacon alert
3	HCF trigger timer
4	NEXT_TIM
5	NEXT_DTIM
6	Quiet time trigger
7	No dedicated function

6.11.65 Generic Timers Mode (MAC_PCU_GENERIC_TIMERS_MODE)

Address: 0x1000_08240
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x00100000

Bit	Name	Description
31:12	THRESH	Number of µs that generate a threshold interrupt if exceeded in TSF comparison
11	RES	Reserved
10:8	OVERFLOW_INDEX	Indicates the last generic timer that overflowed
7:0	ENABLE	Enables the generic timers mode

6.11.66 32 KHz Sleep Mode (MAC_PCU_SLP32_MODE)

Address: 0x1000_08244
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:23	RES	Reserved
22	DISABLE_32KHZ	Indicates the 32 KHz clock is not used to control the TSF, but the MAC clock increments the TSF. Only used on AP class devices that do not go to sleep. Reset Value: 0x0
21	TSF_WRITE_STATUS	The TSF write status. Reset Value: 0x1
20	ENABLE	When set, indicates that the TSF should be allowed to increment on its own. Reset Value: 0x1
19:0	HALF_CLK_LATENCY	Time in µs from the detection of the falling edge of the 32 KHz clk to the rising edge of the 32 KHz clk. Reset Value: 0xF424

6.11.67 32 KHz Sleep Wake (MAC_PCU_SLP32_WAKE)

Address: 0x1000_08248
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x800

Bit	Name	Description
31:16	RES	Reserved
15:0	XTL_TIME	Time in µs before a generic timer should expire that the wake signal asserts to the crystal wake logic. Add an extra 31 µs due to 32 KHz clock resolution.

6.11.68 32 KHz Sleep Increment (MAC_PCU_SLP32_INC)

Address: 0x1000_0824C
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x1E848

Bit	Name	Description
31:20	RES	Reserved
19:0	TSF_INC	Time in $1/2^{12}$ of a µs the TSF increments on the rising edge of the 32 KHz clk (30.5176 µs period). The upper 8 bits are at µs resolution. The lower 12 bits are the fractional portion. $\frac{1\ \text{unit}}{1/2^{12}\ \mu s} = \frac{X}{30.5176\ \mu s}$ Where X = 125000, or 0x1E848 is the default setting for 32.768 MHz clock.

6.11.69 Sleep MIB Sleep Count (MAC_PCU_SLP_MIB1)

Address: 0x1000_08250
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	SLEEP_CNT	Counts the number of 32 KHz clock cycles that the MAC has been asleep

6.11.70 Sleep MIB Cycle Count (MAC_PCU_SLP_MIB2)

Address: 0x1000_08254
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	CYCLE_CNT	Counts the absolute number of 32KHz clock cycles. When CYCLE_CNT bit 31 is 1, the MIB interrupt will be asserted. SLEEP_CNT and CYCLE_CNT are saturating counters when the value of CYCLE_CNT reaches 0xFFFF_FFFF both counters will stop incrementing.

6.11.71 Sleep MIB Control Status (MAC_PCU_SLP_MIB3)

Address: 0x1000_08258
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:2	RES	Reserved
1	PENDING	SLEEP_CNT, CYCLE_CNT, and CLR_CNT are writable for diagnostic purposes. Before every read/write, the pending bit should be polled to verify any pending write has cleared.
0	CLR_CNT	CLR_CNT clears both SLEEP_CNT and CYCLE_CNT. Pending is asserted while the clearing of these registers is pending.

6.11.72 US Scalar (US_SCALAR)

Address: 0x1000_08284
Access: Read/Write
Reset Value: 0x2C

<table>
<tr><th>Bit</th><th>Name</th><th colspan="3">Description</th></tr>
<tr><td>31:7</td><td>RES</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="3">6:0</td><td rowspan="3">US_SCALAR</td><td colspan="3">µs scalar of the MAC clock
Scalar value for generating 1 µs pulses based on the MAC clock.</td></tr>
<tr><td rowspan="2">2.4 GHz</td><td>HT20 mode</td><td>Clock runs at 44 MHz</td></tr>
<tr><td>HT40 mode</td><td>Clock runs at 88 MHz</td></tr>
</table>

6.11.73 Global Mode (MAC_PCU_20_40_MODE)

Address: 0x1000_08318
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:1	RES	Reserved
0	JOINED_RX_CLEAR	Setting this bit causes the rx_clear used in the MAC to be the AND of the control channel rx_clear and the extension channel rx_clear. If this bit is clear then the MAC will use only the control channel rx_clear.

6.11.74 Difference Rx_Clear Counter (MAC_PCU_RX_CLEAR_DIFF_CNT)

Address: 0x1000_08328
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:0	RX_CLEAR_DIFF_CNT	A cycle counter MIB register. On every cycle of the MAC clock, this counter increments every time the extension channel rx_clear is low when the MAC is not actively transmitting or receiving. Due to a small lag between tx_frame and rx_clear as well as between rx_clear and rx_frame, the count may have some residual value even when no activity is on the extension channel.

6.11.75 Control Registers for Block BA Control Fields (MAC_PCU_BA_BAR_CONTROL)

Address: 0x1000_08330
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:10	RES	Reserved
9	ACK_POLICY_VALUE	The value of the ACK policy bit. Reset Value: 0x1
8	COMPRESSED_VALUE	The value of the compressed bit. Reset Value: 0x1
7:4	ACK_POLICY_OFFSET	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the ACK policy bit. Reset Value: 0x0
3:0	COMPRESSED_OFFSET	Indicates the bit offset in the block ACK or block ACK request control field which defines the location of the COMPRESSED bit. Reset Value: 0x2

6.11.76 Legacy PLCP Spoof (MAC_PCU_LEGACY_PLCP_SPOOF)

Address: 0x1000_08334
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: See field description

Bit	Name	Description
31:9	RES	Reserved
12:8	MIN_LENGTH	This register defines the minimum spoofed legacy PLCP length. Reset Value: 0xE
7:0	EIFS_MINUS_DIFS	Defines the number of μs to be subtracted from the transmit packet duration to provide fairness for legacy devices as well as HT devices. Reset Value: 0x0

6.11.77 PHY Error Mask and EIFS Mask (MAC_PCU_PHY_ERROR_MASK_CONT)

Address: 0x1000_08338
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:24	RES	Reserved
23:16	EIFS_VALUE	Continuation of register MAC_PCU_PHY_ERROR_MASK_VALUE. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All others PHY errors above 39 cause EIFS delay.
15:8	RES	Reserved
7:0	MASK_VALUE	Continuation of register MAC_PCU_PHY_ERROR_MASK_VALUE. Bits [2], [1], and [0] correspond to PHY errors 34, 33, and 32. All others PHY errors above 39 will be filtered.

6.11.78 Tx Timer (MAC_PCU_TX_TIMER)

Address: 0x1000_0833C
Access: Hardware = Read/Write
Software = Read/Write
Reset Value: 0x0

Bit	Name	Description
31:16	RES	Reserved
15	TX_TIMER_ENABLE	Enabled when this bit is set to 1.
14:0	TX_TIMER	Guarantees the transmit frame does not take more time than the values programmed in this timer. The unit for this timer is in µs.

6.11.79 MAC Miscellaneous Mode (MAC_MISC_MODE2)

Address: 0x1000_08344
Access: Read/Write

This register is used to set the miscellaneous modes of the MAC, including certain encryptions.

Bit	Bit Name	Type	Reset	Description
31:23	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
22	IGNORE_TXOP_1ST_PKT	R/W	0x1	Setting this bit will allow a single packet to exceed the TXOP
21	CLR_MORE_FRAG	R/W	0x0	Setting this bit will clear the MORE_FRAG signal in the PCU_TXSM. This should be done as a part of the fast channel change. If a fragment burst is terminated before it has completed, this register needs to be set to clear the MORE_FRAG state. If the MORE_FRAG is not cleared, the next fragment burst will ignore the RTS_ENABLE or the RTS_ENABLE located in the descriptor.
20	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
19	DUR_ACCOUNT_BY_BA	R/W	0x1	If this bit is cleared, the duration of the transmit aggregate will assume ACK_SIFS time instead of BA_SIFS time. On transmit of the BA, the duration will be the received aggregate duration minus ACK_SIFS instead of the BA_SIFS. If this bit is set, the duration of the transmit aggregate will use the BA_SIFS time which is required for the MAC to be specifically compliant. On transmit of the BA, the duration will be the receive aggregate duration minus the BA_SIFS.
18	RES	R	0x0	Reserved. Must be written with zero. Contains zeros when read.
17	AGG_WEP	R/W	0x0	Used to set the aggregate encryption 0 — Disables the Improved Encryption Control for Aggregate feature and uses the original control mechanism 1 — Enables the Improved Encryption Control for Aggregate feature
16	EN_LOAD_NAV_BCN_DUR	R/W	0x0	Setting this bit enables the NAV to be updated during the beacon duration
15:8	MGMT_QOS	R/W	0x10	This field indicates the Non-CE Flags Octet field used for management frames for AES_CCM encryption
7	CFP_IGNORE	R/W	0x0	When set the CF parameters set in the information element of beacons are ignored.
6	ADHOC_MCAST_KEYID_EN	R/W	0x1	This field enables the comparison of the KEY ID in the IV field with the value in the keycache. The keycache has a KEY ID field for each adhoc multicast entry. If this bit is not set then the Key ID match is not used to determine whether there is a key search match.

5.4.3 Key Cache (MAC_PCU_KEY_CACHE[0:1023])

Offset: 0x08800
Access: Hardware = Read-Only
Software = Read/Write
Reset Value: 0x0

Table 5-17. **Offset to First Dword of *N*th Key [1]**

Intra Key	Offset Bits	Description	
8*N + 00	31:0	Key[31:0]	
8*N + 04	15:0	Key[47:32]	
8*N + 08	31:0	Key[79:48]	
8*N + 0C	15:0	Key[95:79]	
8*N + 10	31:0	Key[127:96]	
8*N + 14	2:0	Key type:	
		0	40b
		1	104b
		2	TKIP without MIC
		3	128b
		4	TKIP
		5	Reserved
		6	AES_CCM
		7	Do nothing
8*N + 14	14:3	Reserved	
8*N + 18	31:0	Addr[32:1]	
8*N + 1C	14:0	Addr[47:33]	
	15	Key valid	
	17:16	Key ID	

[1]Key = (Address: 8800 + 20*N)

When the key type is 4 (TKIP) and key is valid, this entry + 64 contains the Michael key.

Table 5-18. **Offset to First Dword of *N*th Key (continued)**

Intra Key	Offset Bits	Description
8*N + 800	31:0	Rx Michael key 0
8*N + 804	15:0	Tx Michael key 0 [31:16]
8*N + 808	31:0	Rx Michael key 1
8*N + 80C	15:0	Tx Michael key 0 [15:0]
8*N + 810	31:0	Tx Michael key 1
8*N + 814	RES	Reserved
8*N + 818	RES	Reserved
8*N + 81C	RES	Reserved
	15	Key Valid = 0

TKIP keys are not allowed to reside in the entries 64–127 because they require the Michael key. Entries 64–67 are always reserved for Michael.

NOTE: Internally this memory is 50 bits wide, thus to write a line of the memory requires two 32-bit writes. All writes to registers with an offset of 0x0 or 0x8 actually write to a temporary holding register. A write to register with an offset of 0x4 or 0xC writes to the memory with the current write value concatenated with the temporary holding register.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6-1 summarizes the absolute maximum ratings and Table 6-2 lists the recommended operating conditions for the AR9271.

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 6-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{dd12}	Supply voltage	–0.3 to 1.8	V
V_{dd33}	Maximum I/O supply voltage	–0.3 to 4.0	V
RF_{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T_{store}	Storage temperature	–65 to 150	°C
$T_{junction}$	Junction Temperature	125	°C
ESD	Electrostatic Discharge Tolerance	2000	V
	Electrostatic Discharge Tolerance (RFOUT_N, RFOUT_P, PABIAS and AVDD_XTALI)	1500	V
	Electrostatic Discharge Tolerance (RFIN_P, RFIN_N, XTALO and XTALI)	1200	V

6.2 Recommended Operating Conditions

Table 6-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{dd12}	Supply voltage[1]	±5%	1.14	1.2	1.26	V
V_{dd33}	I/O voltage	±10%	2.97	3.3	3.63	V
T_{case}	Case temperature	—	0	45	110	°C
Psi_{JT}	Thermal Parameter[2]	—	—	—	2.8	°C/W

[1]Since the 1.2 V supply is derived form the 3.3 V supply, the AR9271 expects that the 1.2 V supply lags the 3.3 V supply.
[2]For 8x8 mm LPCC package

6.3 General DC Electrical Characteristics

Table 6-3 lists the GPIO DC electrical characteristics . These conditions apply to all DC characteristics unless otherwise stated.

T_{amb} = 25°C

Table 6-3. **GPIO DC Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	0.7 * V_{dd33}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3 * V_{dd32}	V
V_{OH}	High Level Output Voltage	—	0.9 * V_{dd33}	—	—	V
V_{OL}	Low Level Output Voltage	—	0	—	0.1 * V_{dd33}	V
I_{IL}	Low Level Input Current	—	0	—	26	µA
I_{OH}	High Level Output Current	—	1.8	—	24	mA
I_{OL}	Low Level Output Current	—	-2	—	-31	mA

6.4 USB Pin Characteristics

Table shows the AR9271 USB interface pin characteristics.

Table 6-4. **USB Interface Characteristics**

Signal Name	Pin	Type	Drive	PU/DP Resistance
USB Interface Characteristics				
DP	38	IA/OA	—	—
TXRTUNE	39	IA/OA	—	—
DM	40	IA/OA	—	—
GPIO Interface Characteristics				
GPIO_0 to GPIO_15	12, 18, 19, 20, 21, 23, 28, 29, 30, 31, 35, 36, 44, 45, 48, 49	I/O	Up to 24 mA	250 KΩ PU

6.5 EEPROM Timing Specifications

Table defines the timing parameters for the EEPROM interface while Figure shows the timing for the EEPROM interface.

Table 6-5. **EEPROM Timing Parameters**

Symbol	Parameter	Min	Max	Unit
T_{sck}	EPRM_SCK Cycle Time	4	—	µs
T_{high}	High Time of EPRM_SCK (Parameter Scales with T_{sck})	0.35 * T_{sck}	0.40 * T_{sck}	µs
T_{w_val}	Write Data Valid from Falling Edge EPRM_SCK (parameter Scales with T_{sck})	0.10 * T_{sck}	0.15 * T_{sck}	µs
T_{r_su}	Read Data Setup Time to Rising Edge of EPRM_SCK	50	—	ns
T_{r_h}	Read Data Hold time from Rising Edge of EPRM_SCK	50	—	ns

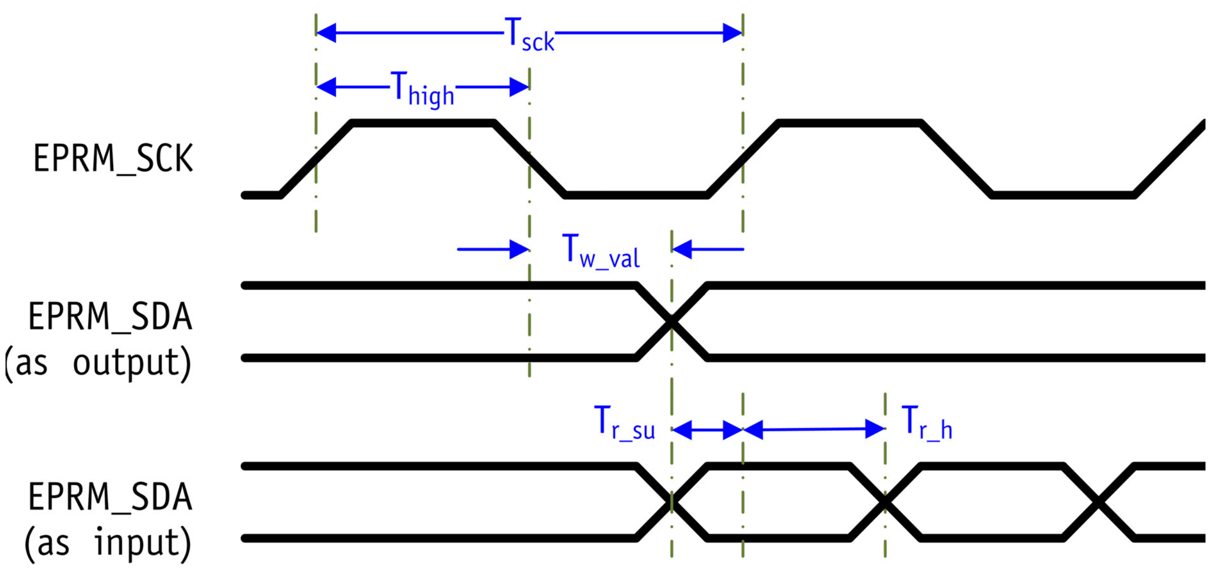


Figure 6-1. **EEPROM Timing**

6.6 Radio Receiver Characteristics

Table 6-6 summarizes the AR9271 receiver characteristics.

Table 6-6. **Radio Receiver Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{rx}	Receiver input frequency range	5 MHz center frequency	2.412	—	2.472	GHz
NF	Receive chain noise figure (max gain)	LNA2 (dedicated Rx)	—	3.5	—	dB
		LNA1 (Tx/Rx shared)	—	5.5	—	
S_{rf}	Sensitivity[1]					
	CCK, 1 Mbps	See Note[2]	-80	-96	—	dBm
	CCK 11 Mbps		-76	-89	—	
	OFDM, 6 Mbps		-82	-92	—	
	OFDM, 54 Mbps		-65	-76	—	
	HT20, MCS0, 1 stream, 1 Tx, 1 Rx	See Note[2]	-82	-92	—	
	HT20, MCS7, 1 stream, 1 Tx, 1 Rx		-64	-73	—	
	HT40, MCS0, 1 stream 1 Tx, 1 Rx	See Note[2]	-79	-88	—	
	HT40, MCS7, 1 stream 1 Tx, 1 Rx		-61	-70	—	
IP1dB	Input 1 dB compression (min. gain)	—	—	-7	—	
IIP3	Input third intercept point (min. gain)	—	—	1	—	
Z_{RFin_input}	Recommended LNA differential drive impedance	LNA2	—	36+j13	—	Ω
ER_{phase}	I, Q phase error	—	—	1.0[3]	—	°
ER_{amp}	I, Q amplitude error	—	—	0.3[3]	—	dB
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	10 to 20 MHz[4]	16	37	—	dB
	OFDM, 54 Mbps		-1	22	—	
	HT20, MCS0		16	37	—	
	HT20, MCS7		-2	20	—	
TR_{powup}	Time for power up (from synthesizer)	—	—	1.5	—	µs

[1]Sensitivity for LNA2 (Rx only chain). Sensetivity for LNA1 (Rx/Tx shared chain) is 3 dB worse than LNA2.
[2]Sensetivity performance based on Atheros reference design, which includes a Tx/Rx antenna switch. Minimum values based on IEEE 802.11 specifications.
[3]IQ Phase Error and IQ Amplitude Error are analog values prior to digital correction.
[4]Typical values measured with reference design. Minimum values based on IEEE 802.11 specifications.

6.7 Radio Transmitter Characteristics

Table 6-7 summarizes the transmitter characteristics of the AR9271.

Table 6-7. **Transmitter Characteristics for 2.4 GHz Operation**

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		5 MHz center frequency	2.412	—	2.472	GHz
P_{out}	Mask Compliant CCK output power (1M, Long Preamble)		See Note[1]	—	19	—	dBm
	EVM Compliant OFDM output power for 64 QAM		See Note[1]	—	18	—	dBm
	HT20 – MCS7		—	—	17	—	dBm
	HT40 – MCS7			—	16	—	
SP_{gain}	PA gain step		See Note[2]	—	0.5	—	dB
A_{pl}	Accuracy of power leveling loop		See Notes[3][4]	—	±0.5	—	dB
Z_{RFout_load}	Recommend differential PA load impedance		See Note[5]	—	17+j5	—	Ω
OP1dB	Output P1dB (max. gain)		2.442 GHz	—	12	—	dBm
OIP3	Output third order intercept point (max. gain)		2.442 GHz	—	23	—	dBm
SS	Sideband suppression		—	—	–38	—	dBc
RS	Synthesizer reference spur		—	—	–70	—	dBc
Tx_{mask}	Transmit spectral mask						
	OFDM	At 11 MHz offset	See Note[6]	—	–28	–20	dBr
		At 22 MHz offset		—	–40	–28	
		At 30 MHz offset		—	–51	–40	
	HT20	At 11 MHz offset		—	–26	–20	dBr
		At 22 MHz offset		—	–42	–28	
		At 30 MHz offset		—	–49	–40	
	HT40	At 21 MHz offset		—	–25	–20	dBr
		At 40 MHz offset		—	–36	–28	
		At 60 MHz offset		—	–51	–45	
TT_{powup}	Time for power up (from synthesizer on)		—	—	1.5	—	µs

[1]Measured using the balun recommended by Atheros under closed-loop power control.
[2]Guaranteed by design.
[3]Manufacturing calibration required.
[4]Not including tolerance of external power detector and its temperature variation.
[5]See the impedance matching circuit in the Atheros reference design schematics. To achieve good RF performance, it is strongly recommended not to alter the RF portion of the Atheros reference design for different matching networks.
[6]Measured at the antenna connector port. Average conducted transmit power levels = 17 dBm for 802.11b, 802.11g, HT20 and16 dBm for HT40. Maximum values based on IEEE 802.11 specifications.

6.8 Synthesizer Characteristics

Table 6-8 summarizes the synthesizer characteristics for the AR9271.

Table 6-8. **Synthesizer Composite Characteristics for 2.4 GHz Operation**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pn	Phase noise (at Tx_Out)					
	At 30 KHz offset		—	–93	—	dBc/Hz
	At 100 KHz offset		—	–91	—	
	At 500 KHz offset		—	–101	—	
	At 1 MHz offset		—	–114	—	
F_c	Center channel frequency	Center frequency at 5 MHz spacing[1]	2.412	—	2.484	GHz
F_{ref}	Reference oscillator frequency	± 20 ppm[2]	—	40	—	MHz
TS_{powup}	time for power up	—	—	200	—	µs

[1]Frequency is measured at the Tx output.
[2]Over temperature variation and aging.

6.9 Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

V_{dd2} = 1.2 V
V_{dd3} = 3.3 V, Tamb = 25 °C

Table 6-9 shows the typical power drain as a function of the AR9271's operating mode.

Table 6-9. **Power Consumption for 2.4 GHz Operation[1][2][3][4]**

Mode	Operating Mode	3.3 V Supply (mA)	1.2V Supply (mA)
HT40	Sleep	0	2
	Tx	330	132
	Rx	56	160
HT20	Sleep	0	2
	Tx	340	112
	Rx	55	111
802.11g	Sleep	0	2
	Tx	340	112
	Rx	55	111
802.11b	Sleep	0	2
	Tx	340	93
	Rx	55	100

[1]Values in this table include integrated PA, LNA and LDO.
[2]For Tx, transmitter and synthesizer are on. Tx power at 17 dBm for 801.11b/802.11g/HT20 and 16 dBm for HT40.
[3]For Tx, transmitter and synthesizer are on. Tx power at 18 dBm for 802.11b/g/HT20 and 16 dBm HT40.
[4]For Rx, receiver and synthesizer are on with maximum receiver gain.

7. LDO Circuit Recommendation

The AR9271 can be powered by an optional on-chip LDO. Along with an external PNP, this block provides a regulated 1.2 V power supply for the rest of the AR9271. Figure 7-1 displays a diagram with recommended components for the AR9271 low dropout regulator.

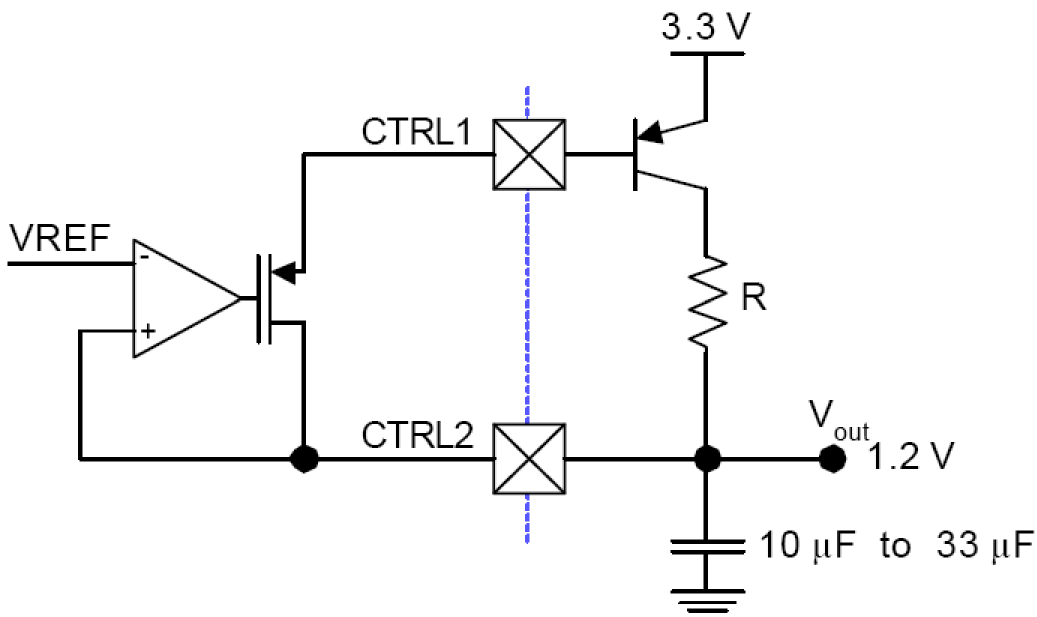


Figure 7-1. **AR9271 Low Dropout Regulator**

If the on-chip LDO is not used, the CTRL1 pin should be pulled down to ground by 10 kohm resistor to disable the internal amplifier.

7.1 PNP Transistor

When selecting the PNP transistor, power dissipation of the transistor should be considered. The PNP collector can be connected to a series resistor (R) for sharing the load of power dissipation with the PNP. The size of the resistor depends on the power rating. For example, it can be a 2.2 Ω or two 4.7 Ω resistors connected in parallel between the collector and the capacitor. The LDO should provide power to the AR9271 only.

8. Package Dimensions

The AR9271 LPCC-68 package drawings and dimensions are provided in Figure 8-1 and Figure 8-2 and in Table 8-1 and Table 8-2.

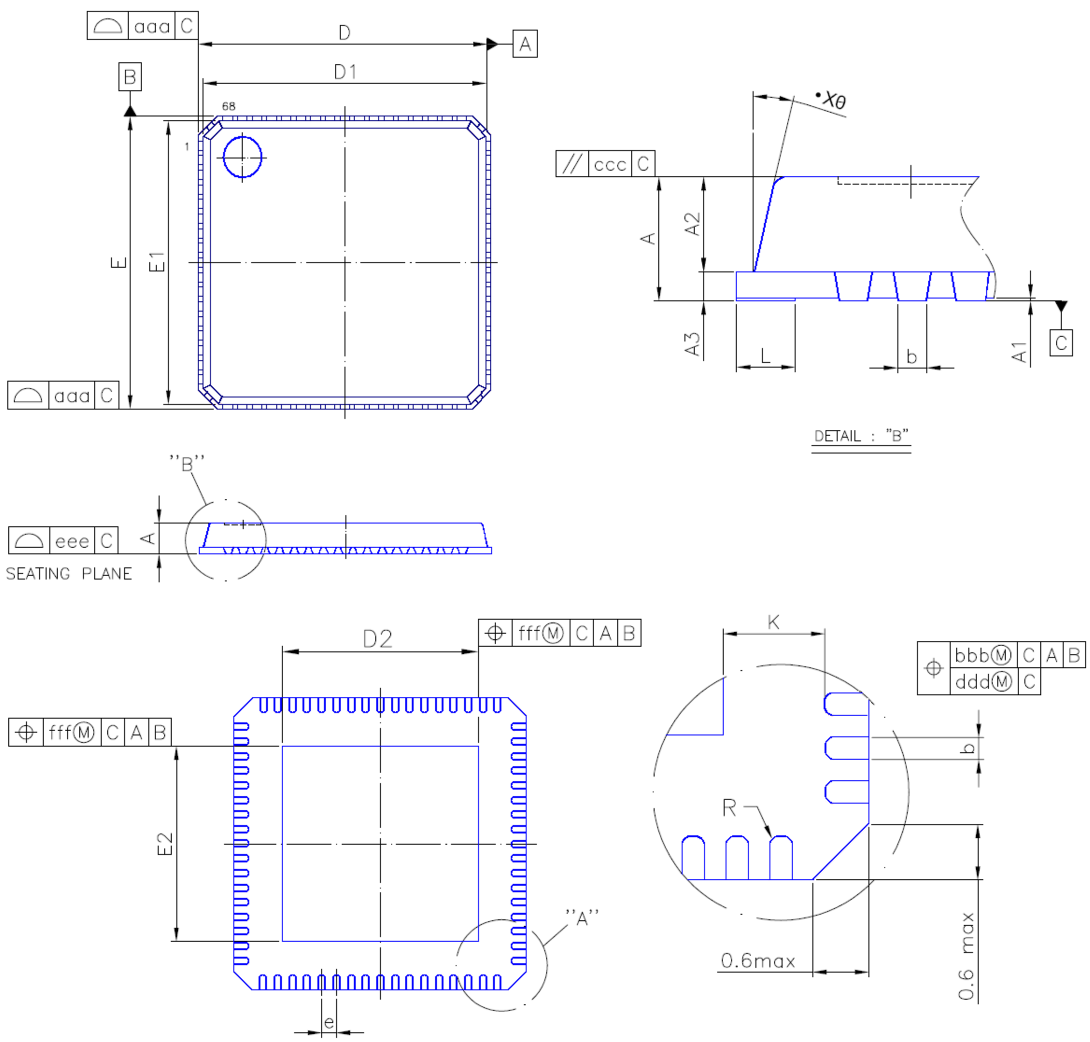


Figure 8-1. **Package Details**

Table 8-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	1.00	mm	0.031	0.033	0.039	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.80	mm	0.024	0.026	0.031	inches
A3	0.20 REF			mm	0.008 REF			inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	8.00 BSC			mm	0.315 BSC			inches
D1/E1	7.75 BSC			mm	0.305BSC			inches
D2/E2	5.33	5.84	6.35	mm	0.209	0.229	0.250	inches
e	0.40 BSC			mm	0.016 BSC			inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
θ	0°	—	14°C	degrees	32°F	—	57°F	degrees
R	0.075	—	—	mm	0.003	—	—	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa	—	—	0.10	mm	—	—	0.004	inches
bbb	—	—	0.07	mm	—	—	0.003	inches
ccc	—	—	0.10	mm	—	—	0.004	inches
ddd	—	—	0.05	mm	—	—	0.002	inches
eee	—	—	0.08	mm	—	—	0.003	inches
fff	—	—	0.10	mm	—	—	0.004	inches

[1]Controlling dimension: Millimeters
[2]Reference document: JEDEC MO-220

The AR9271 chip design also includes a sawed-type packaging. Please reference Table 8-2 and Figure 8-2 to better understand the differences between these two types of packaging.

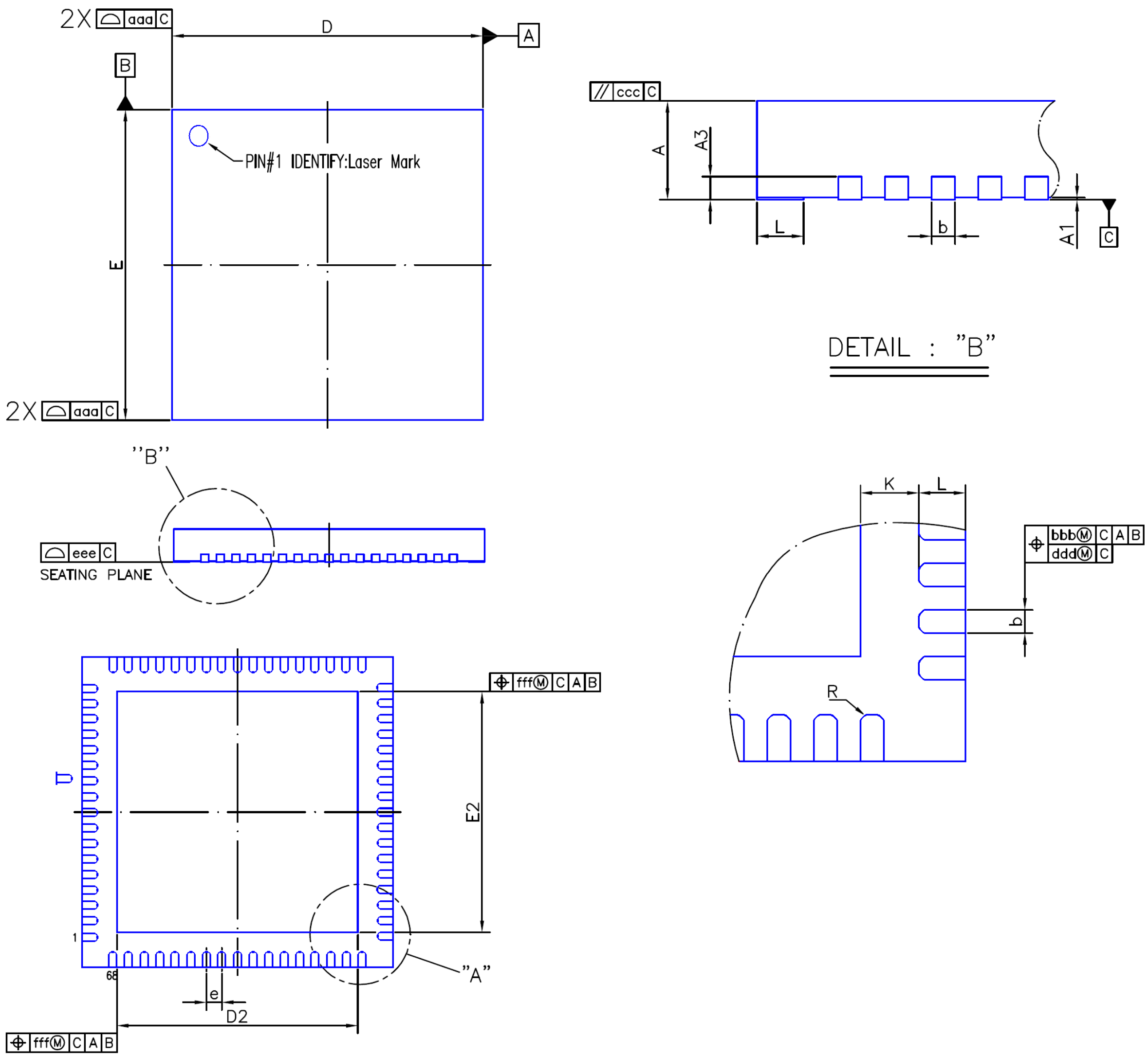


Figure 8-2. **Sawed-type Package Details**

Table 8-2. **Sawed-Type Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.031	0.033	0.035	inches
A1	0.00	0.02	0.05	mm	0.000	0.001	0.002	inches
A3	0.20 REF			mm	0.008 REF			inches
b	0.15	0.20	0.25	mm	0.006	0.008	0.010	inches
D/E	7.90	8.00	8.10	mm	0.311	0.315	0.319	inches
D2	5.33	5.84	6.35	mm	0.209	0.229	0.250	inches
E2	5.33	5.84	6.35	mm	0.209	0.229	0.250	inches
e	0.40 BSC			mm	0.016 BSC			inches
L	0.30	0.40	0.50	mm	0.012	0.016	0.020	inches
R	0.075	—	—	mm	0.003	—	—	inches
K	0.20	—	—	mm	0.008	—	—	inches
aaa	0.10			mm	0.004			inches
bbb	0.07			mm	0.003			inches
ccc	0.10			mm	0.004			inches
ddd	0.05			mm	0.002			inches
eee	0.08			mm	0.003			inches
fff	0.10			mm	0.004			inches

[1]Controlling dimension: Millimeters
[2]Reference document: JEDEC MO-220

9. Ordering Information

The order number AR9271-AL3A specifies a lead-free standard-temperature version of the AR9271.

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Atheros assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any updates. Atheros reserves the right to make changes, at any time, to improve reliability, function or design and to attempt to supply the best product possible.

Document Number: MKG-0955 Ver. 3.0

Atheros Communications, Incorporated
1700 Technology Drive
San Jose, CA 950110
t: 408/773-5200
f: 408/773-9940
www.atheros.com