The DM9000 is a fully integrated and cost-effective single chip Fast Ethernet MAC controller with a general processor interface, a 10/100M PHY and 4K Dword SRAM. It is designed with low power and high performance process that support 3.3V with 5V tolerance.

The DM9000 also provides a MII interface to connect HPNA device or other transceivers that support MII interface. The DM9000 supports 8-bit, 16-bit and 32-bit uP interfaces to internal memory accesses for different processors. The PHY of the DM9000 can interface to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9000 to take the maximum advantage of its abilities. The DM9000 also supports IEEE 802.3x full-duplex flow control. This programming of the DM9000 is very simple, so user can port the software drivers to any system easily.

**Block Diagram**
Specifications

- Supports processor interface: byte/word/dword of I/O command to internal memory data operation
- Integrated 10/100M transceiver
- Supports MII and reverses MII interface
- Supports back pressure mode for half-duplex mode flow control
- IEEE802.3x flow control for full-duplex mode
- Supports wakeup frame, link status change and magic packet events for remote wake up
- Integrated 4K dword SRAM

- Supports automatically load vendor ID and product ID from EEPROM
- Supports 4 GPIO pins
- Optional EEPROM configuration
- Very low power consumption mode:
  - Power reduced mode (cable detection)
  - Power down mode
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.
- Compatible with 3.3V and 5.0V tolerant I/O
- 100-pin LQFP with CMOS process

Application

VoIP CPE (ATA, IP Phone, Video Phone)
IP STB, IPC, Internet Radio

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Pin Count</th>
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<tbody>
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<td>DM9000E</td>
<td>100</td>
<td>LQFP</td>
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<tr>
<td>DM9000EP</td>
<td>100</td>
<td>LQFP (Pb-Free)</td>
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</tbody>
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